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MITANI (43) **Pub. Date: Jul. 2, 2020**

(54) **DISPLAY DEVICE**

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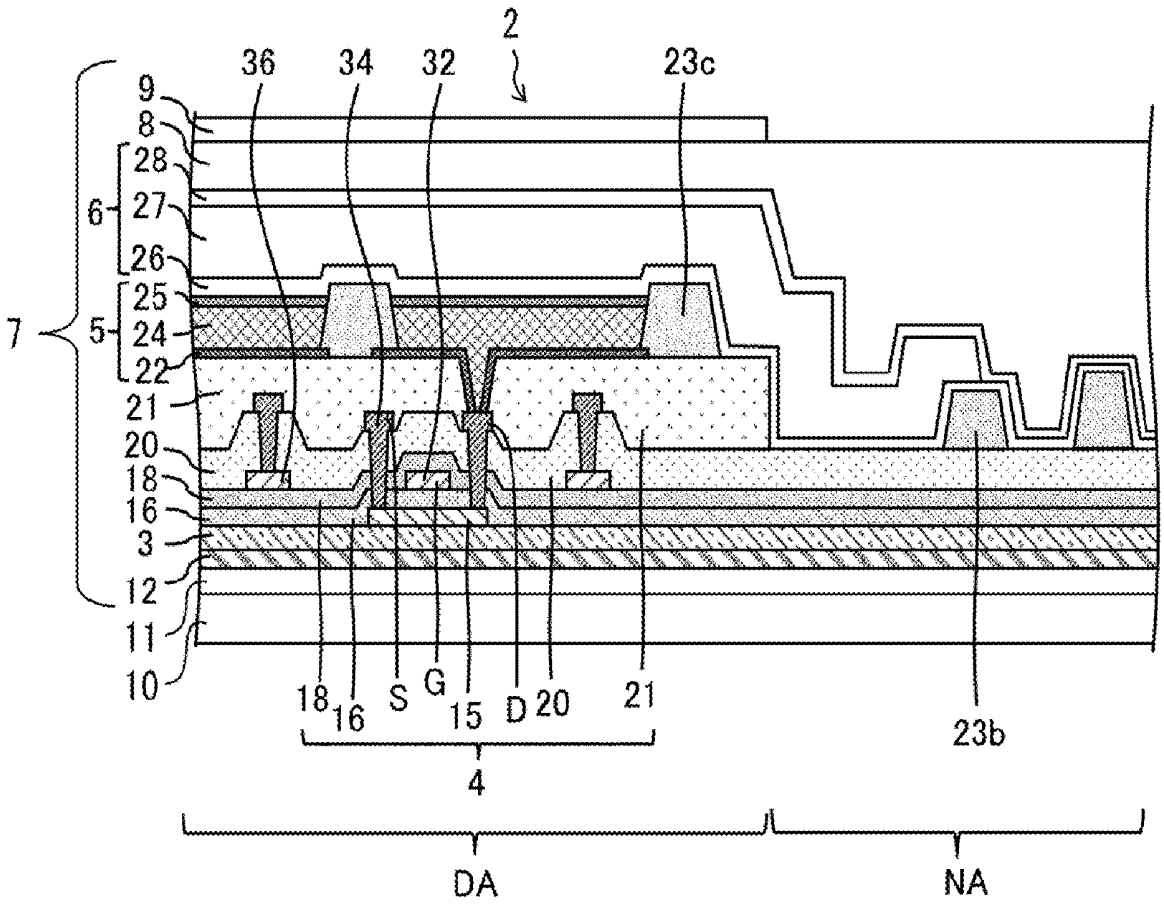
CPC ***H01L 27/3276*** (2013.01); ***H01L 51/0097*** (2013.01)

(57) **ABSTRACT**

An active side slit and an FPC side slit each extend through a second inorganic insulating film and reach a first inorganic insulating film. The active side slit is formed between an active region and an IC chip mounted region of an EL device in plan view and also, the IC chip mounted region is sandwiched between the active side slit and the FPC side slit.



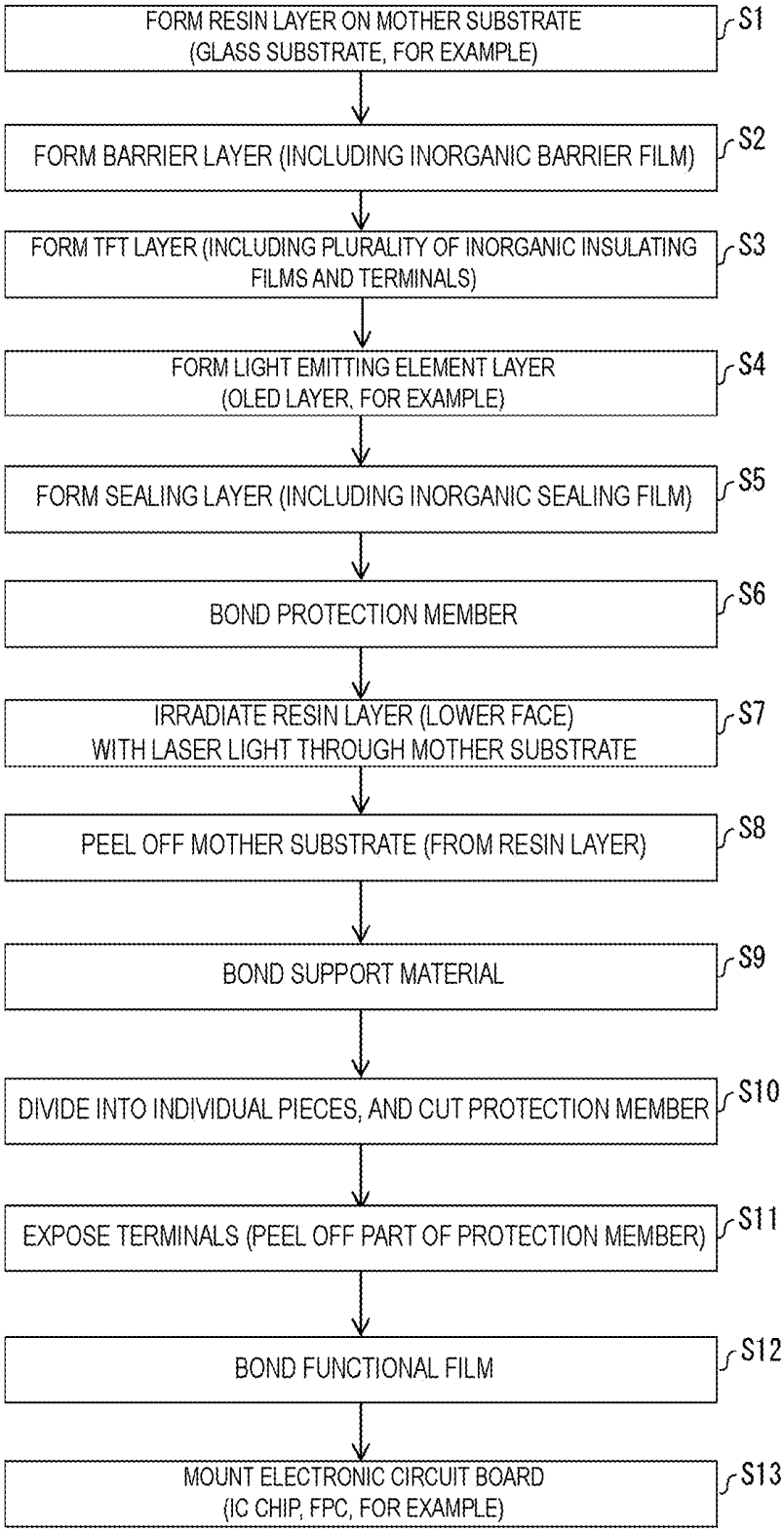

FORM RESIN LAYER ON MOTHER SUBSTRATE (GLASS SUBSTRATE, FOR EXAMPLE)
S1
FORM BARRIER LAYER (INCLUDING INORGANIC BARRIER FILM)
S2
FORM TFT LAYER (INCLUDING PLURALITY OF INORGANIC INSULATING FILMS AND TERMINALS)
S3
FORM LIGHT EMITTING ELEMENT LAYER (OLED LAYER, FOR EXAMPLE)
S4
FORM SEALING LAYER (INCLUDING INORGANIC SEALING FILM)
S5
BOND PROTECTION MEMBER
S6
IRRADIATE RESIN LAYER (LOWER FACE) WITH LASER LIGHT THROUGH MOTHER SUBSTRATE
S7
PEEL OFF MOTHER SUBSTRATE (FROM RESIN LAYER)
S8
BOND SUPPORT MATERIAL
S9
DIVIDE INTO INDIVIDUAL PIECES, AND CUT PROTECTION MEMBER
S10
EXPOSE TERMINALS (PEEL OFF PART OF PROTECTION MEMBER)
S11
BOND FUNCTIONAL FILM
S12
MOUNT ELECTRONIC CIRCUIT BOARD (IC CHIP, FPC, FOR EXAMPLE)
S13

FIG. 1

FIG. 2A

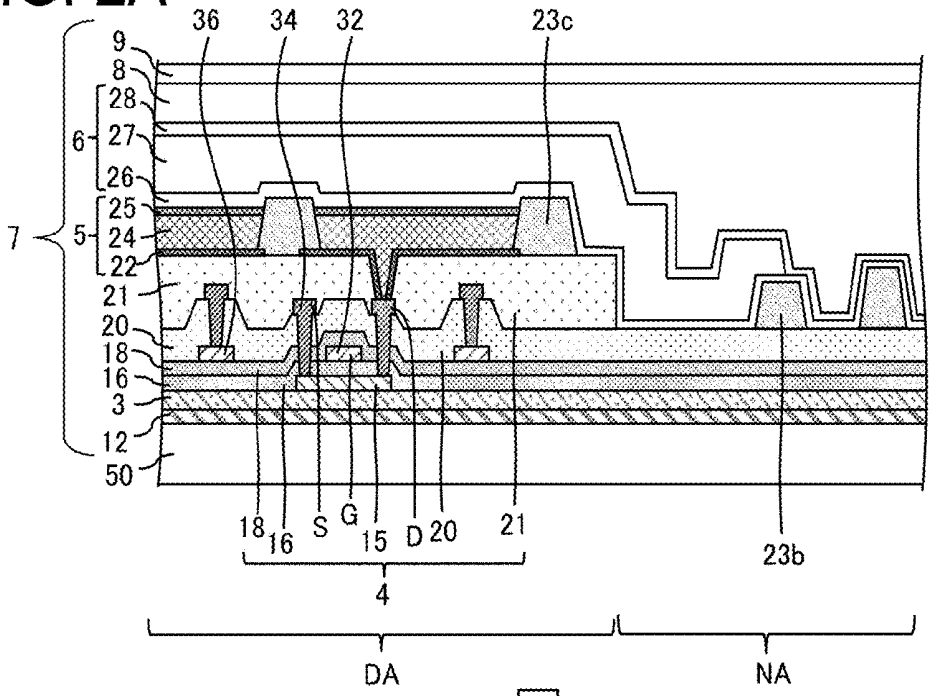

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FIG. 2B

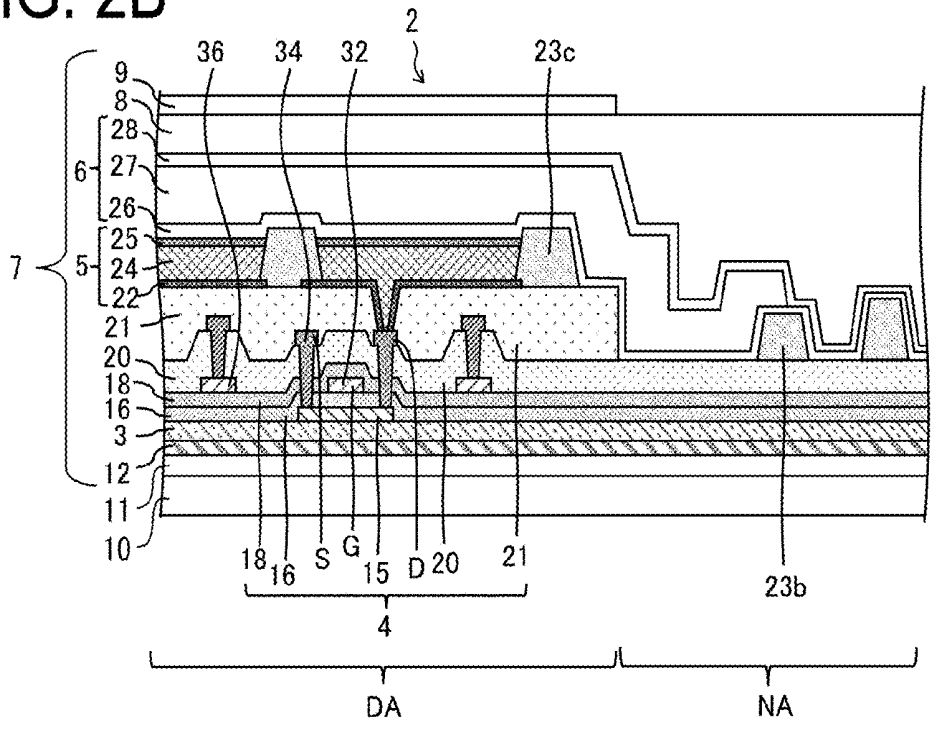
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FIG. 3A

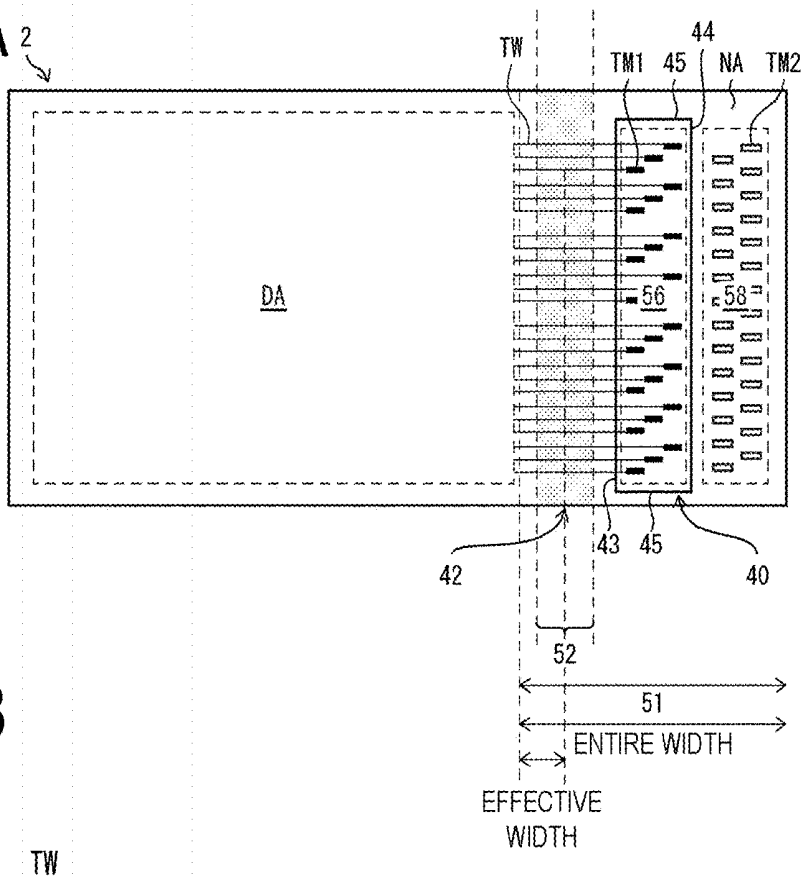
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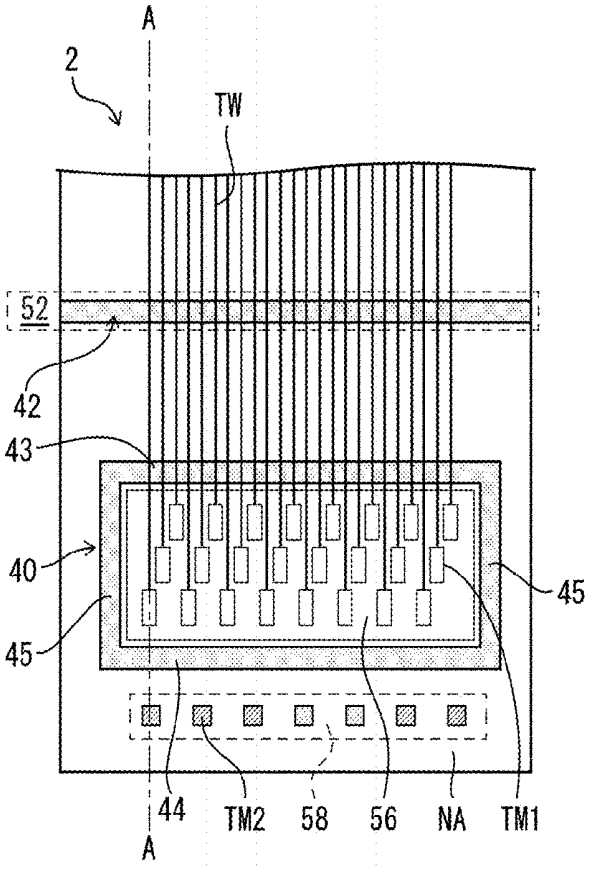
FIG. 3B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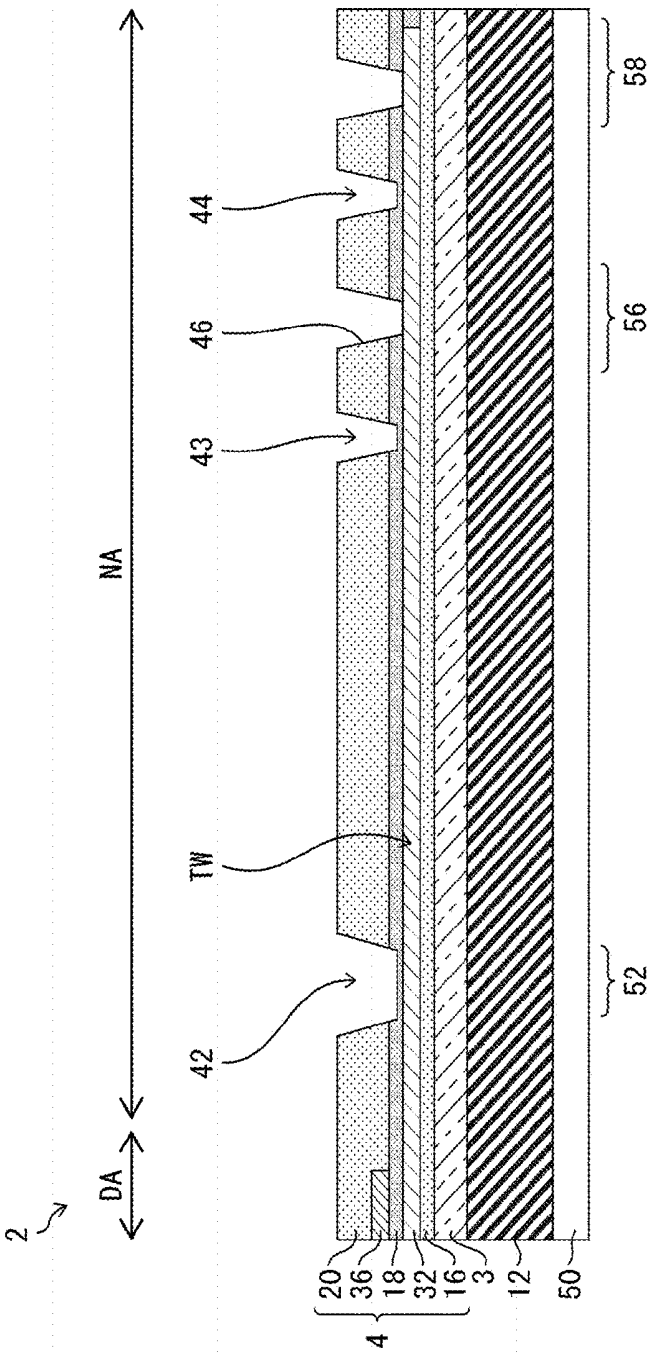

FIG. 4

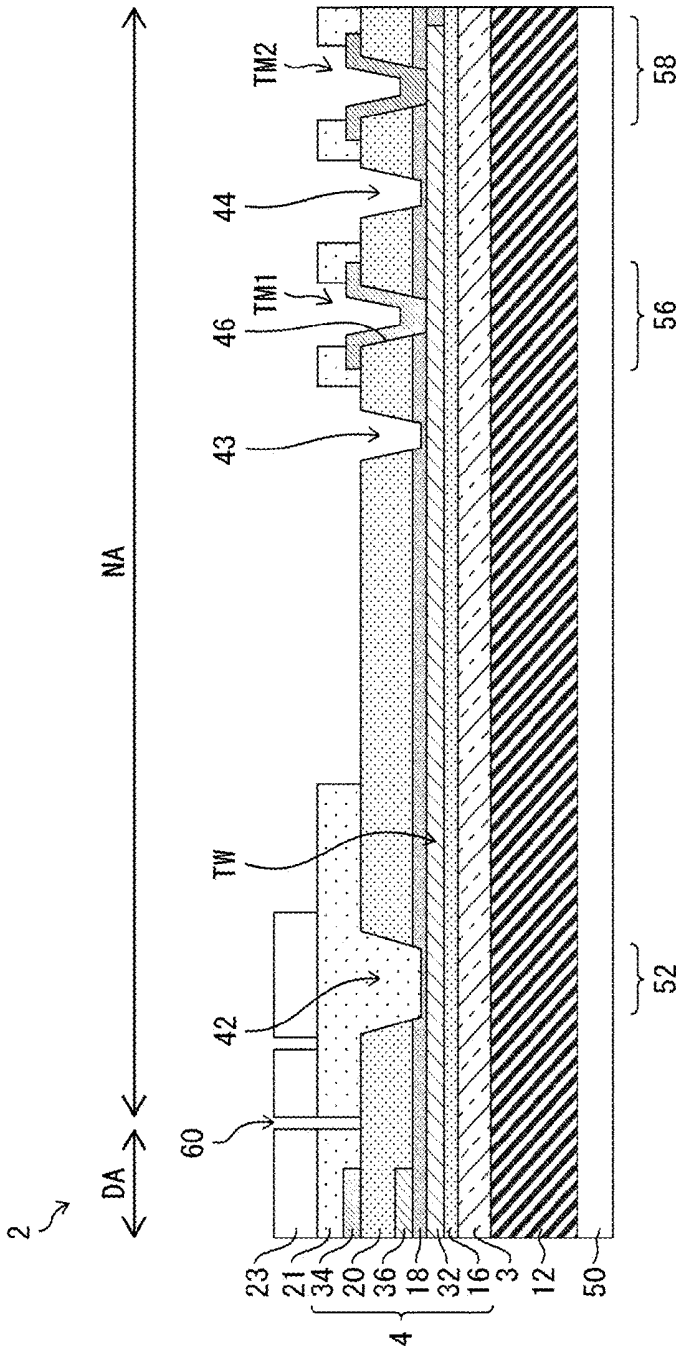
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FIG. 5

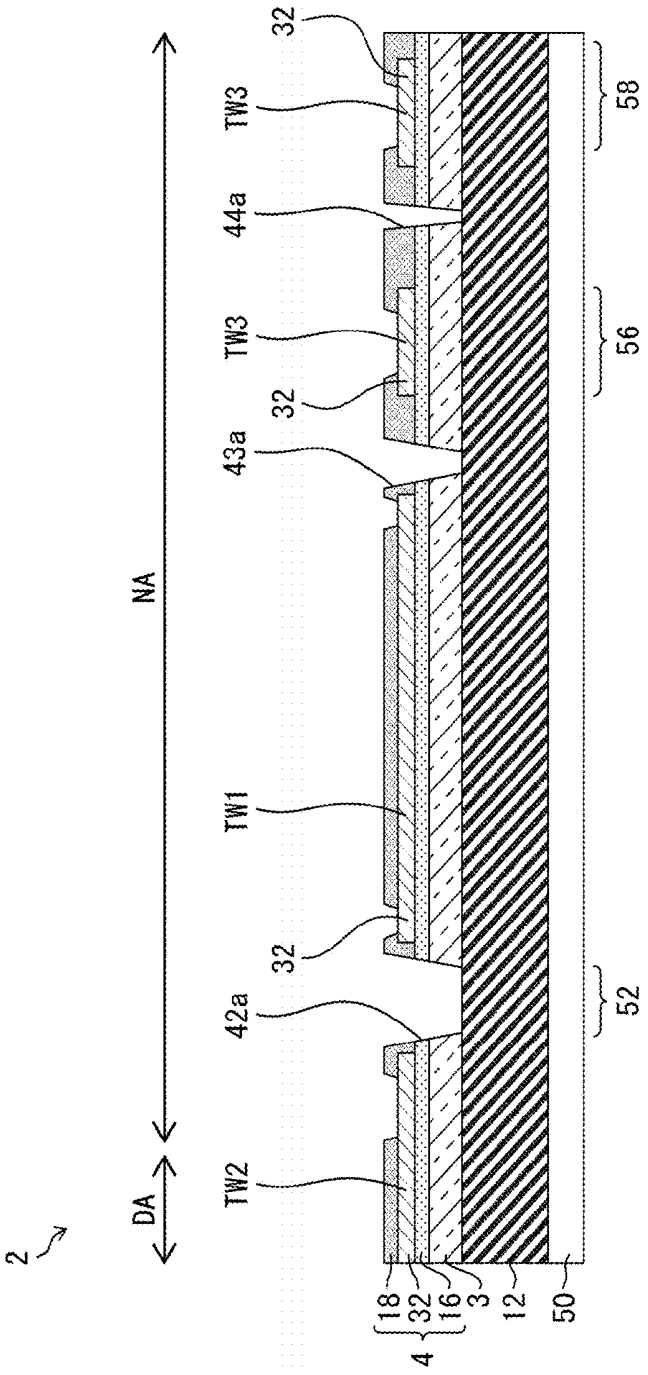
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FIG. 6

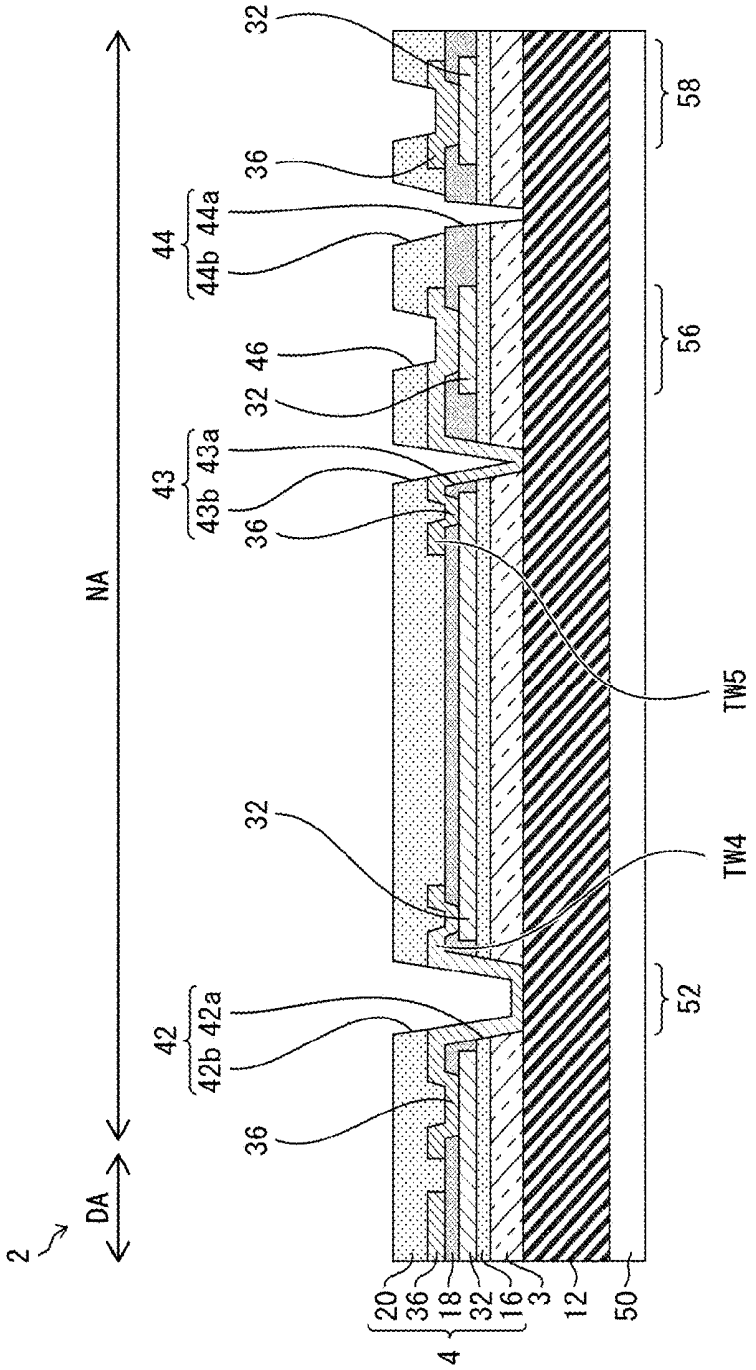
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FIG. 7

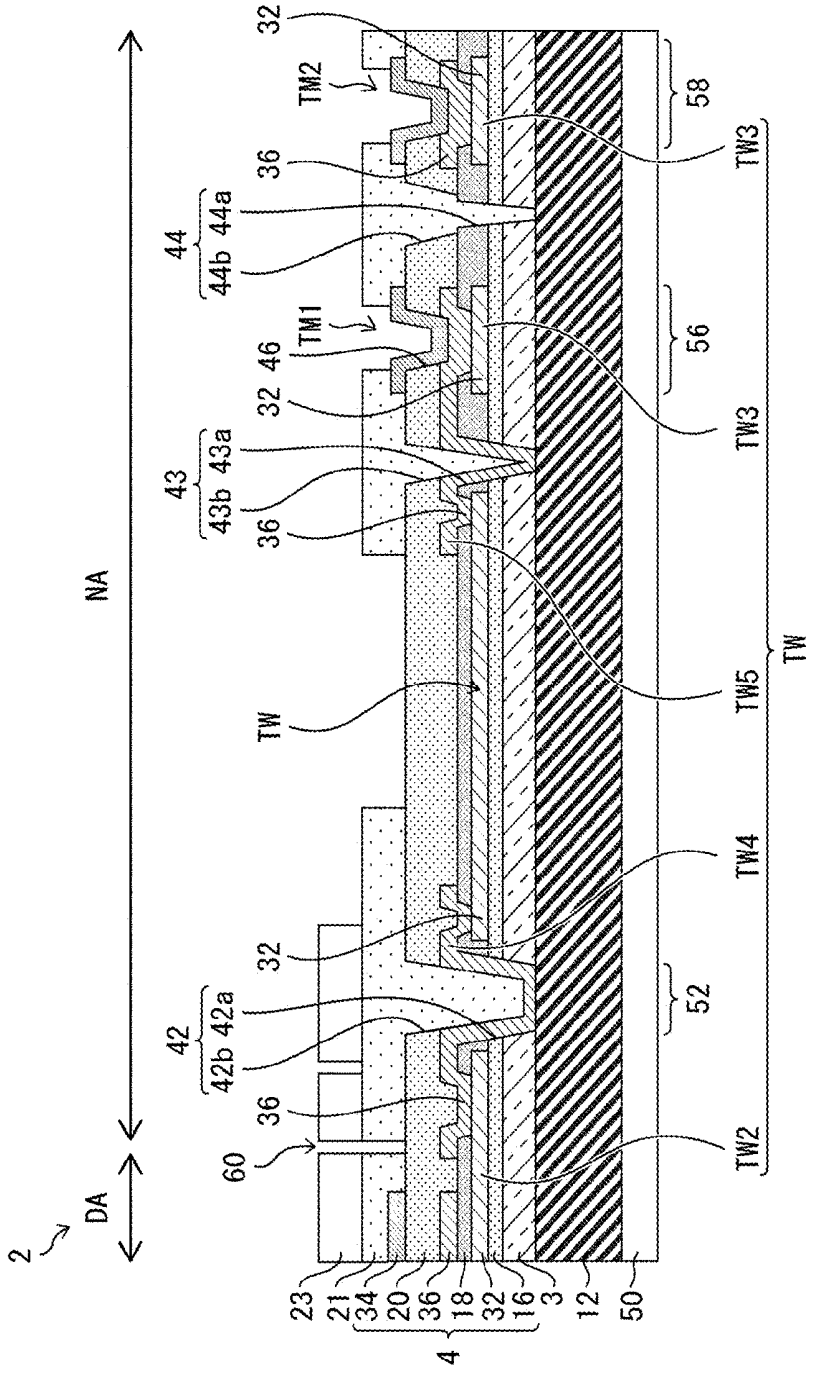
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FIG. 8

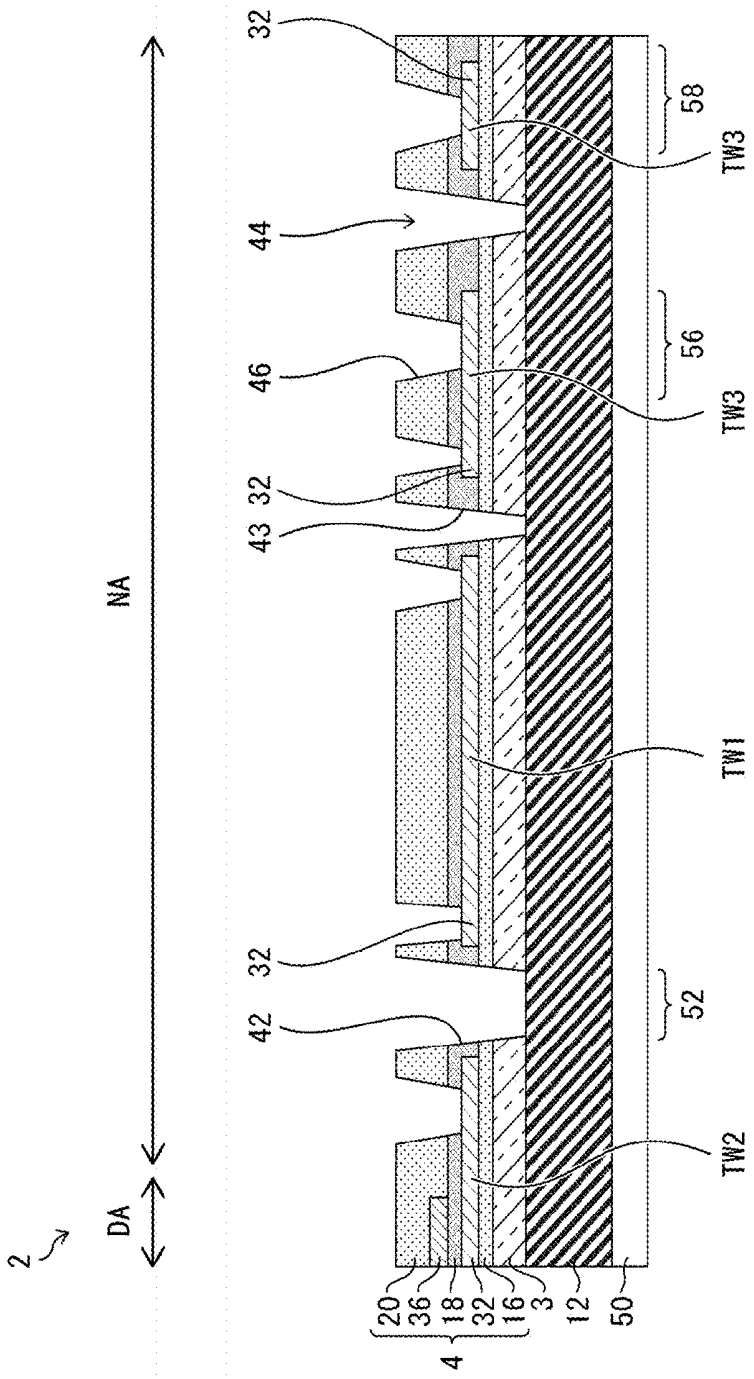
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FIG. 9

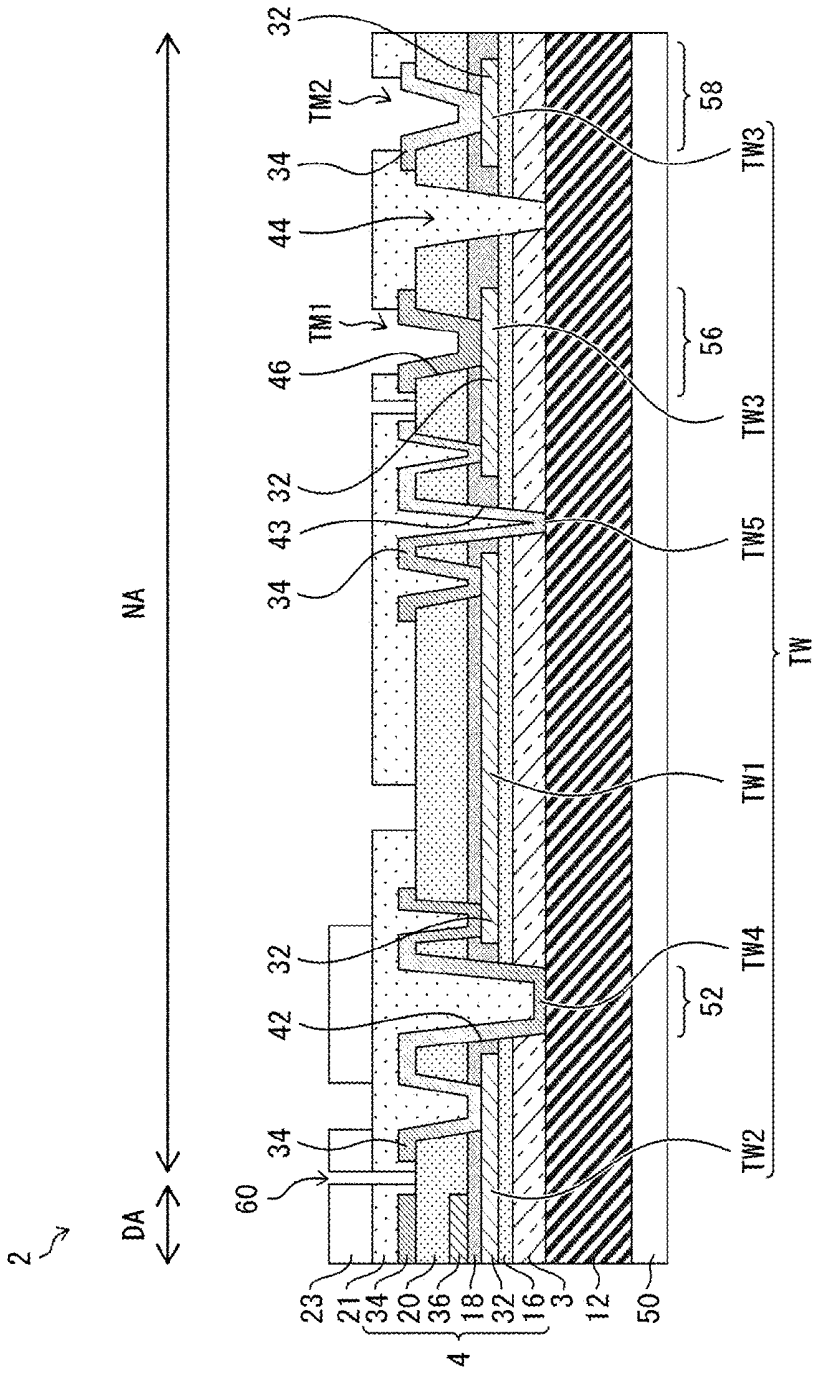
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FIG. 10

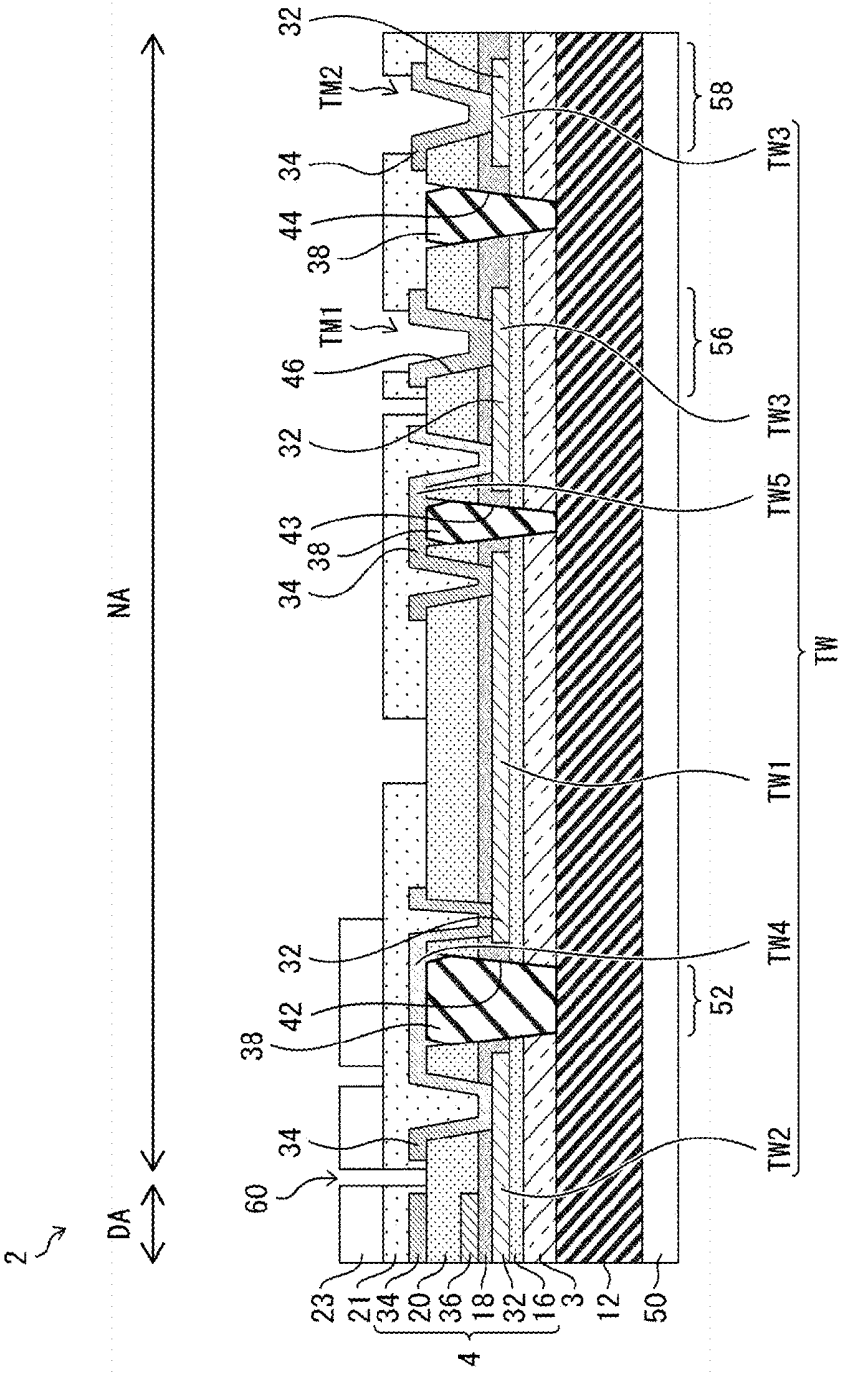
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FIG. 11

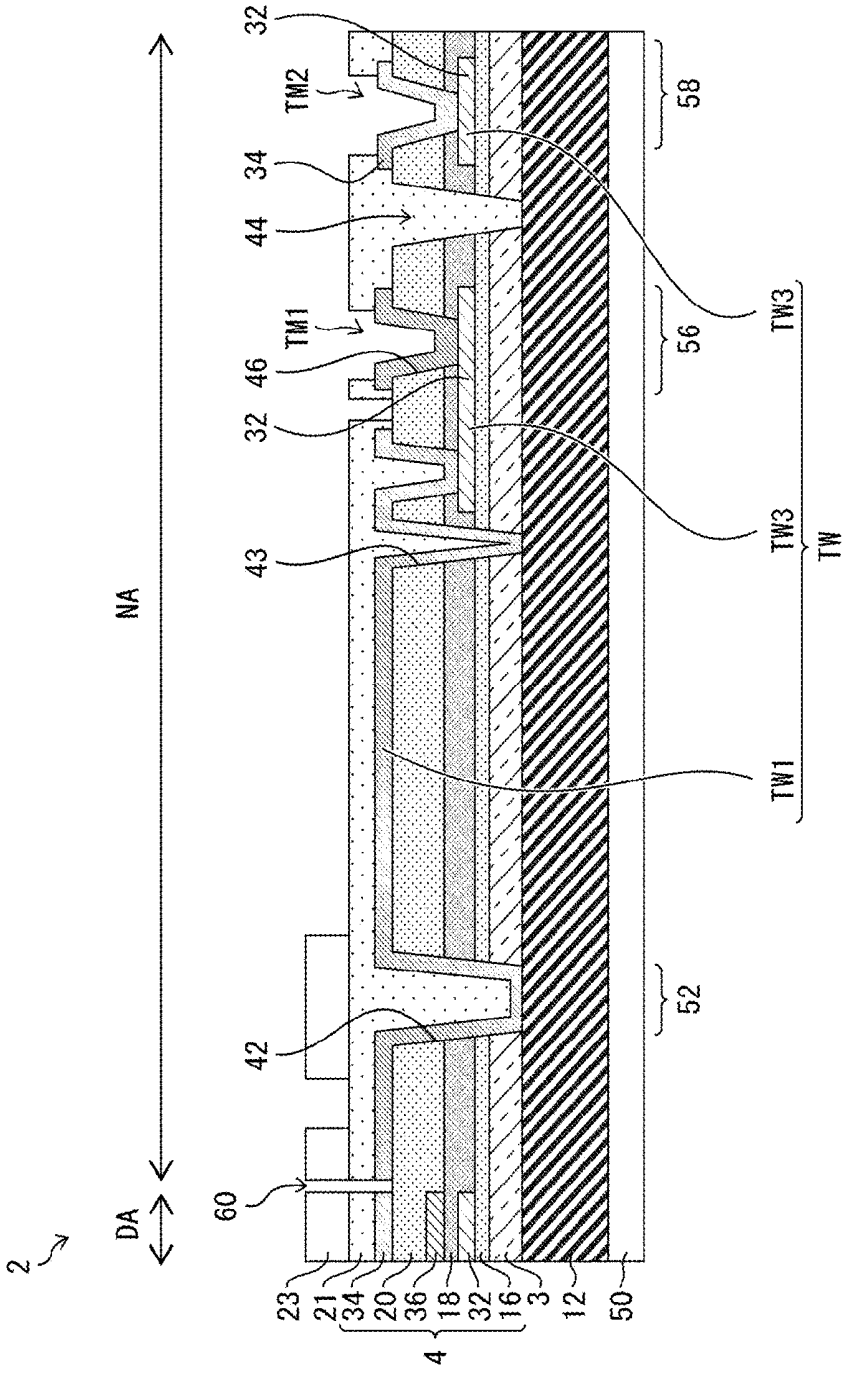
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FIG. 12

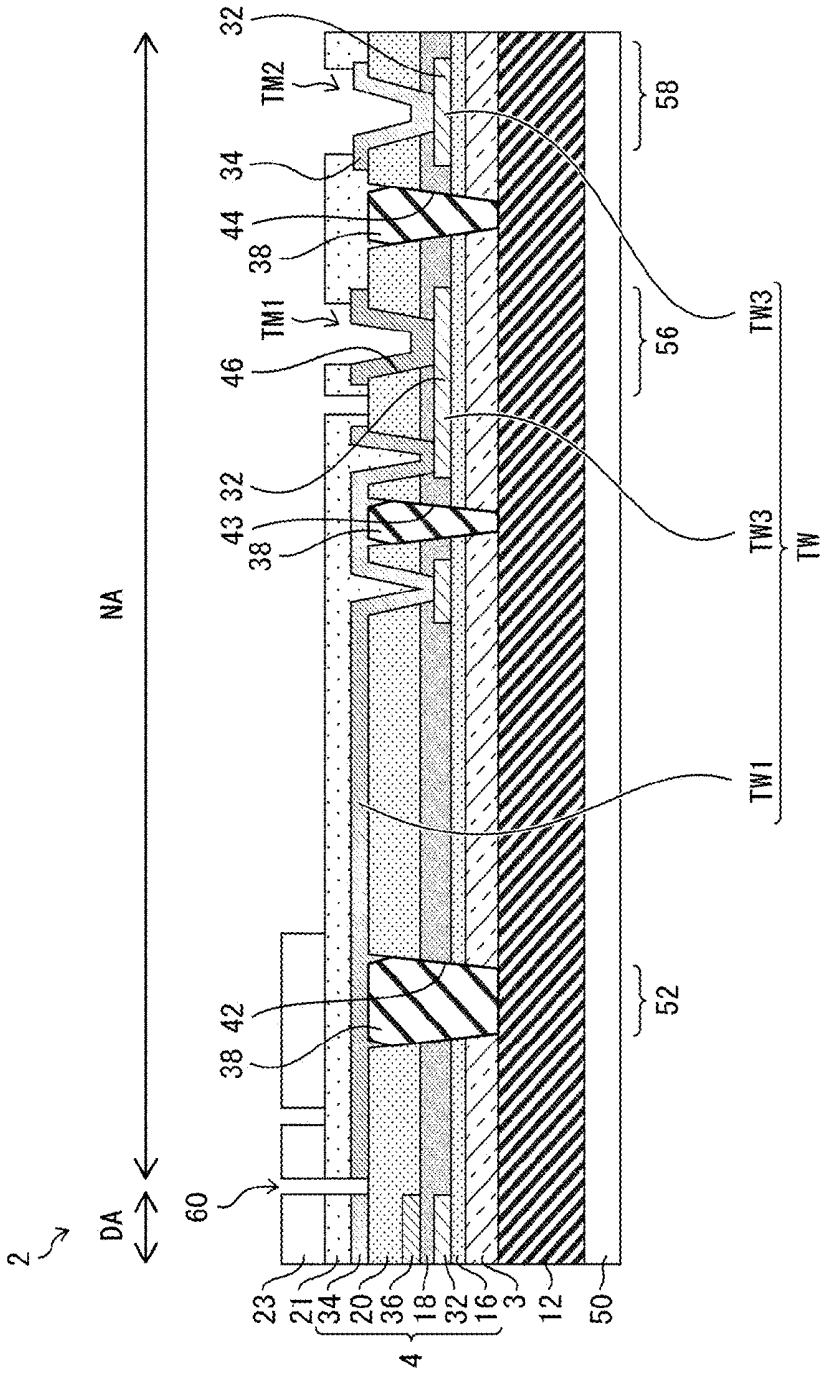
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FIG. 13

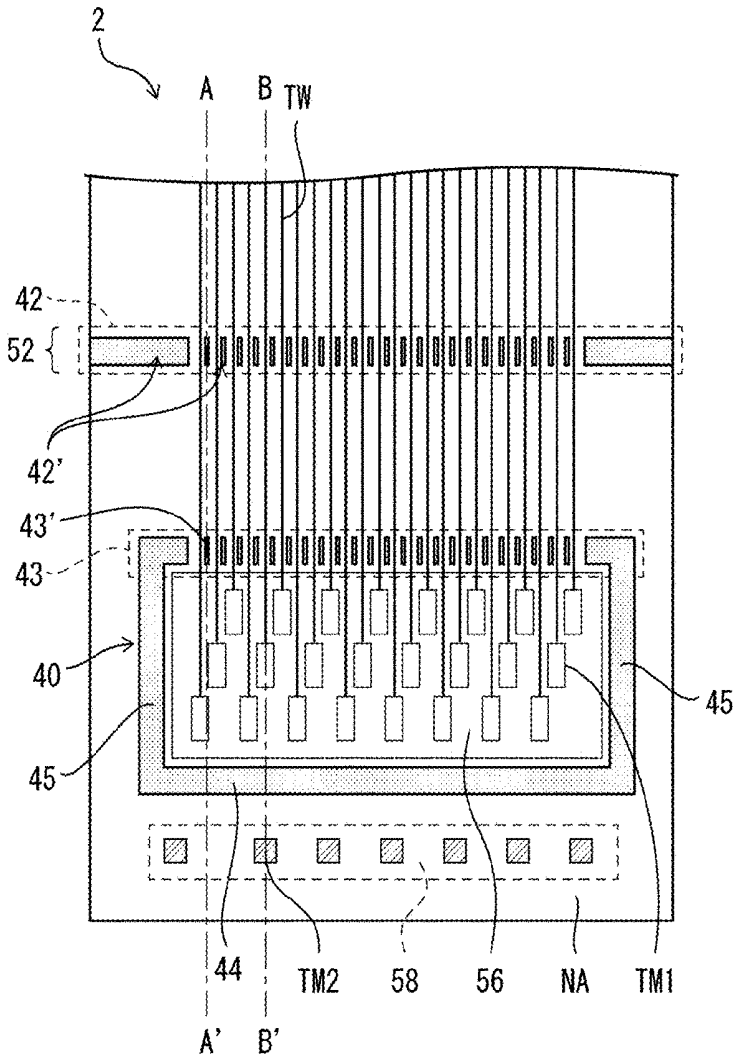

FIG. 14

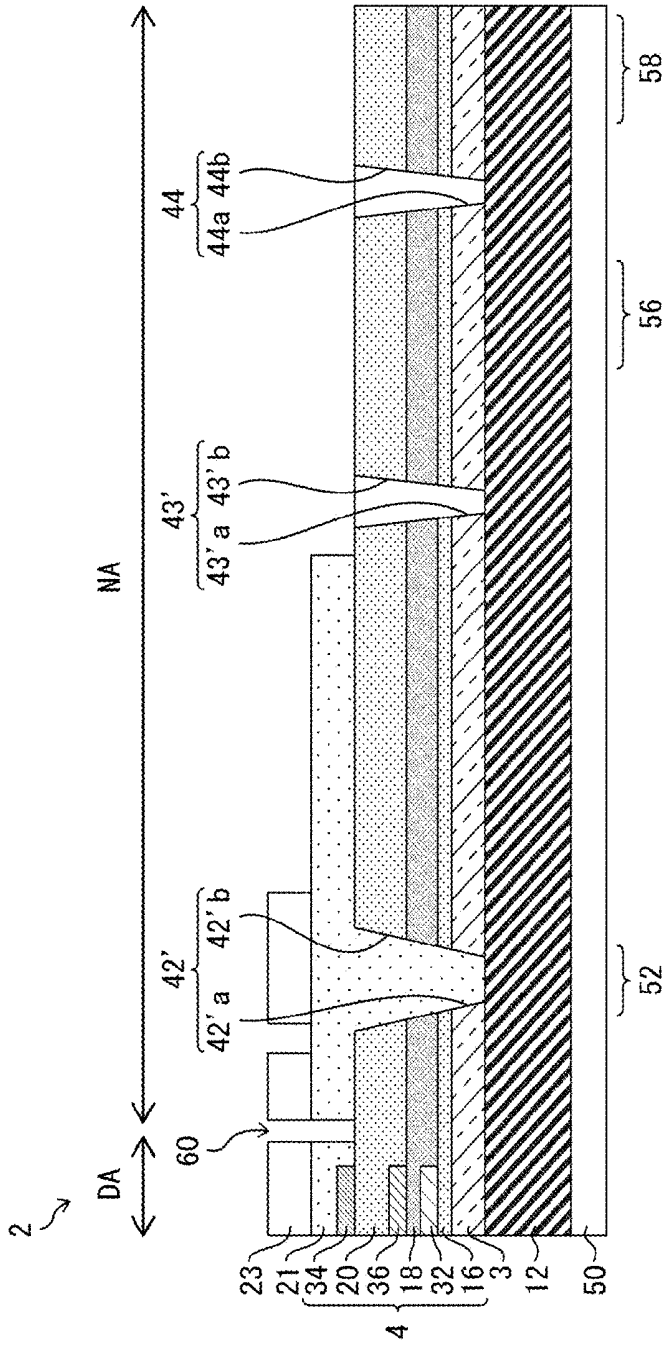
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FIG. 15

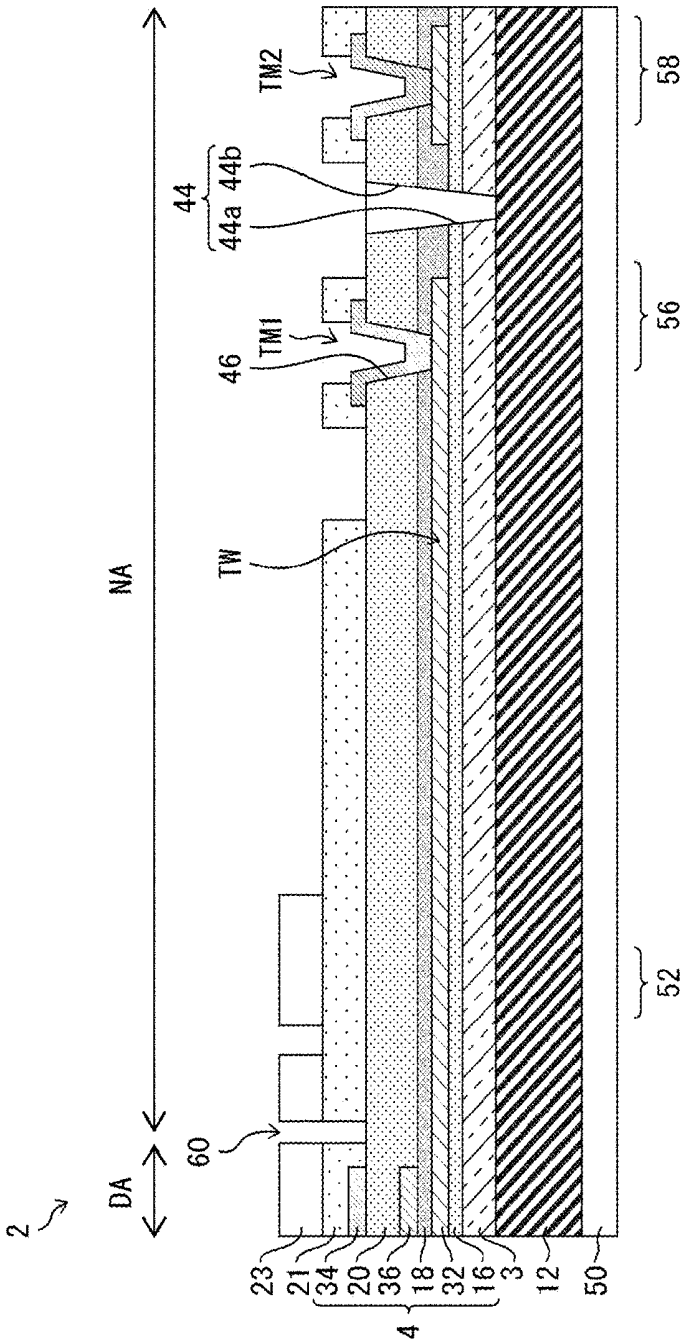
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FIG. 16

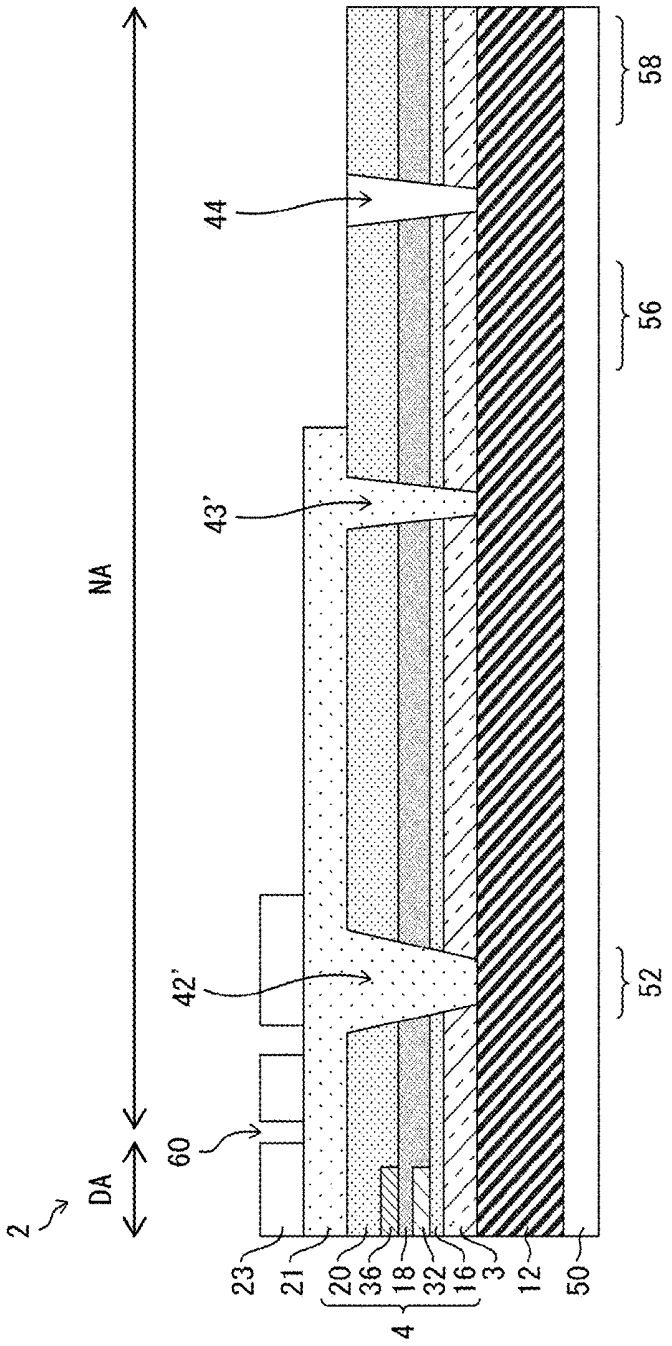

FIG. 17

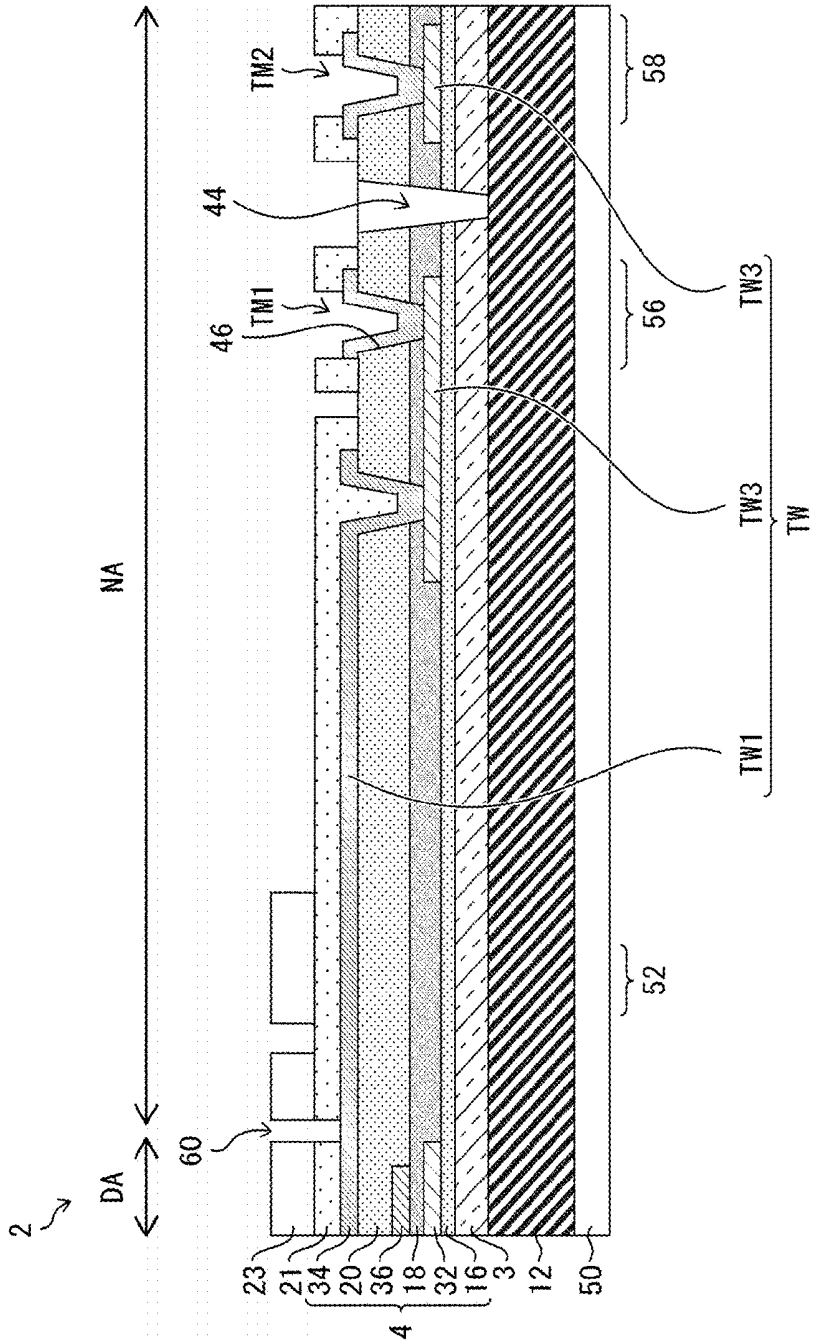
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FIG. 18

FIG. 19A

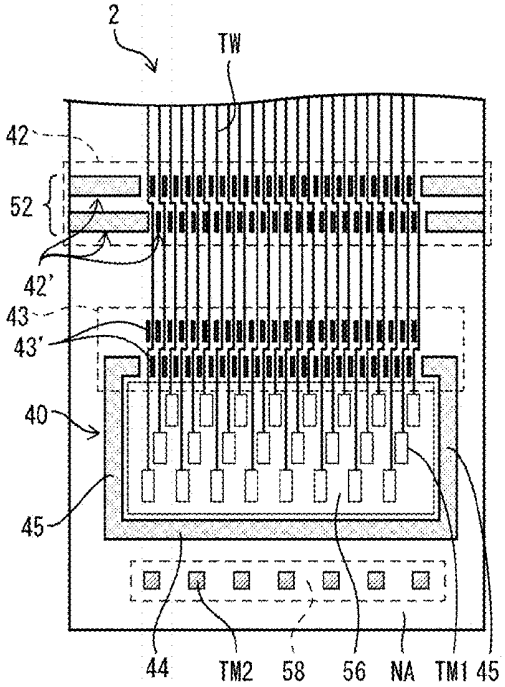


FIG. 19B

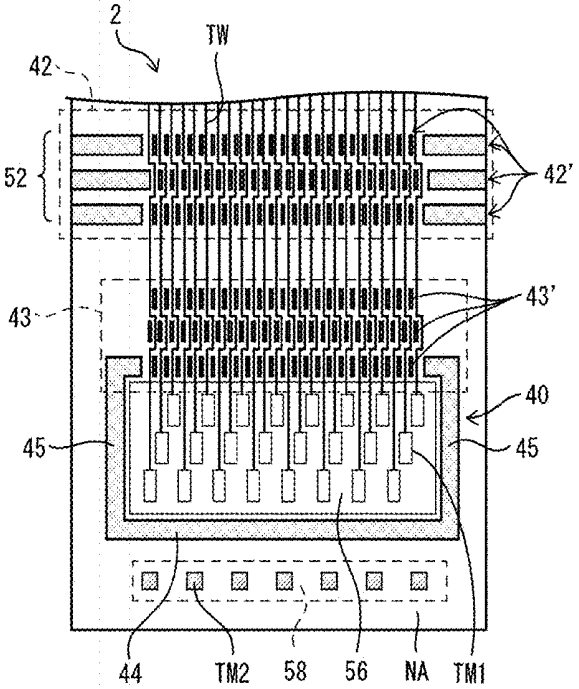


FIG. 19C

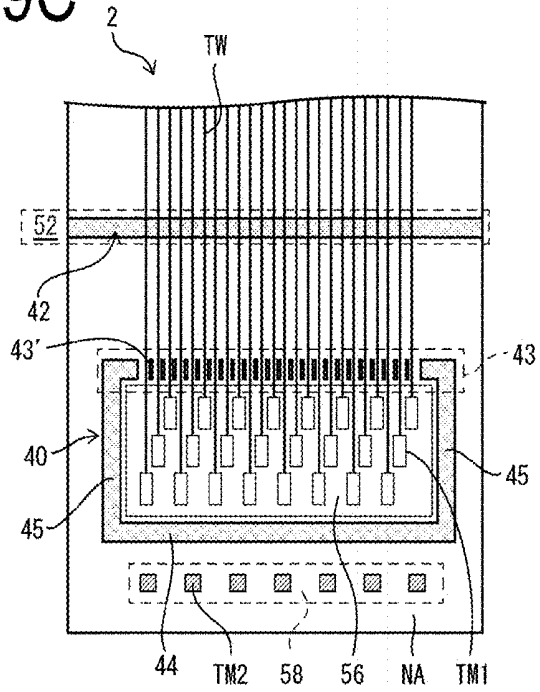


FIG. 20A

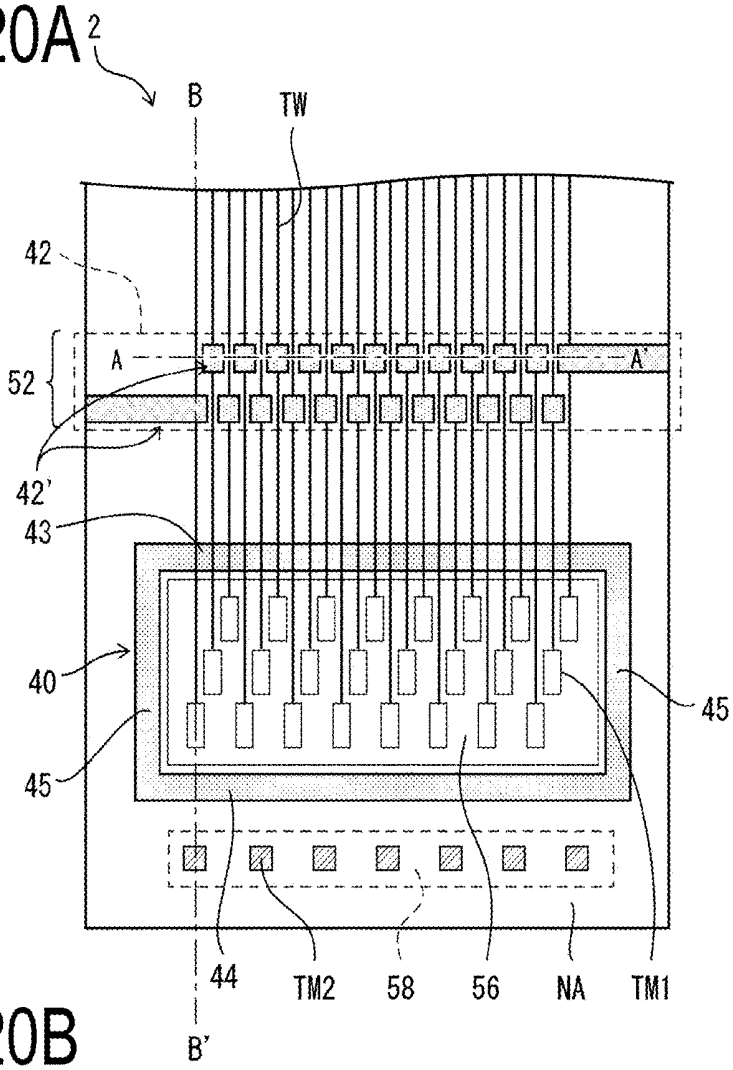
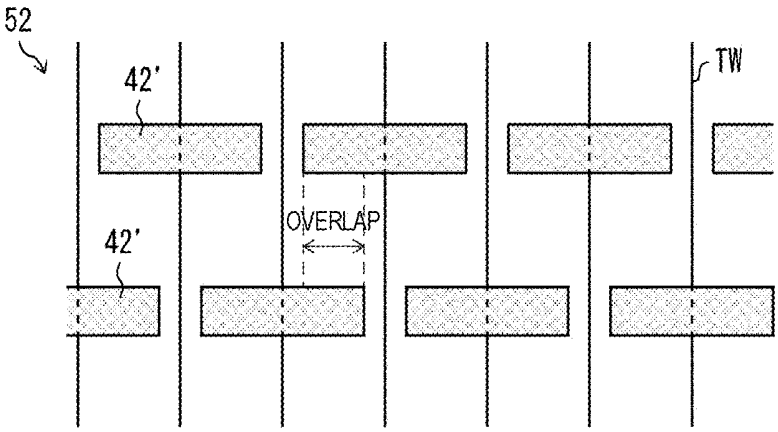


FIG. 20B



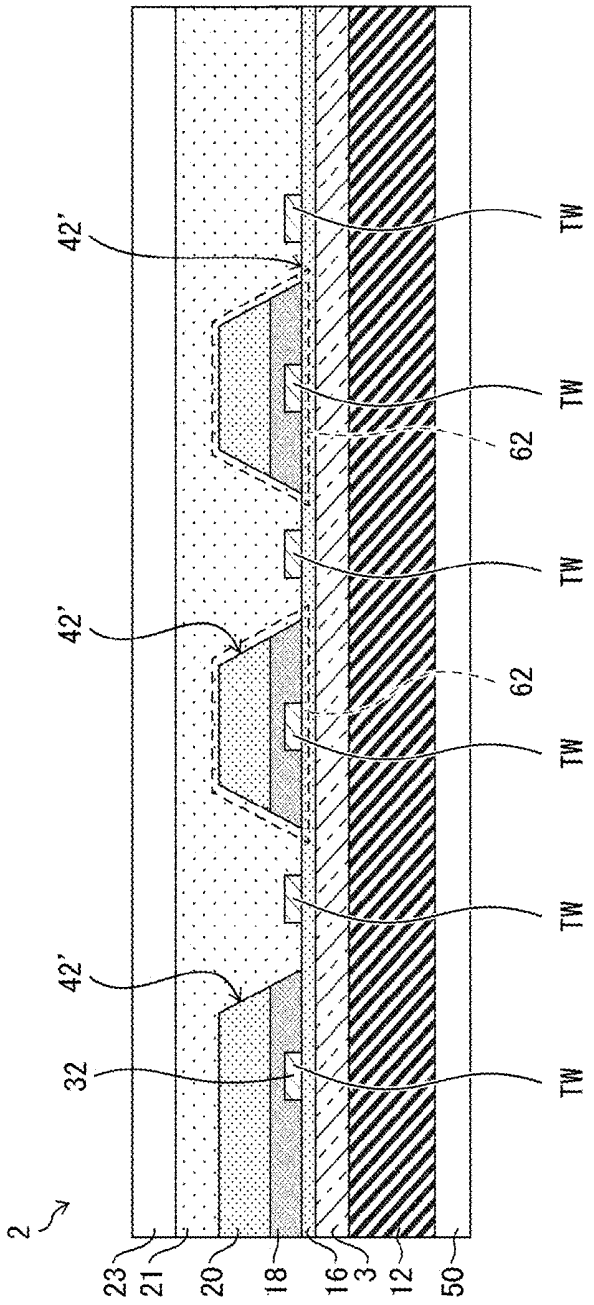


FIG. 21

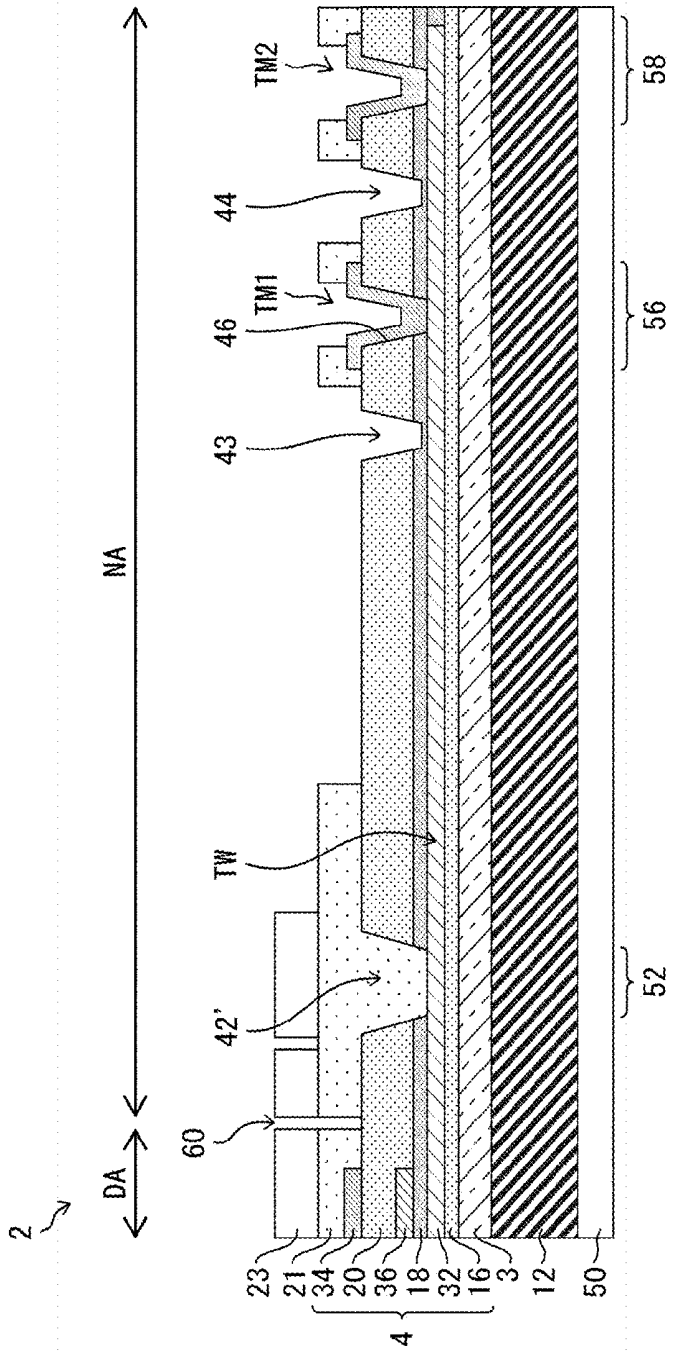

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FIG. 22

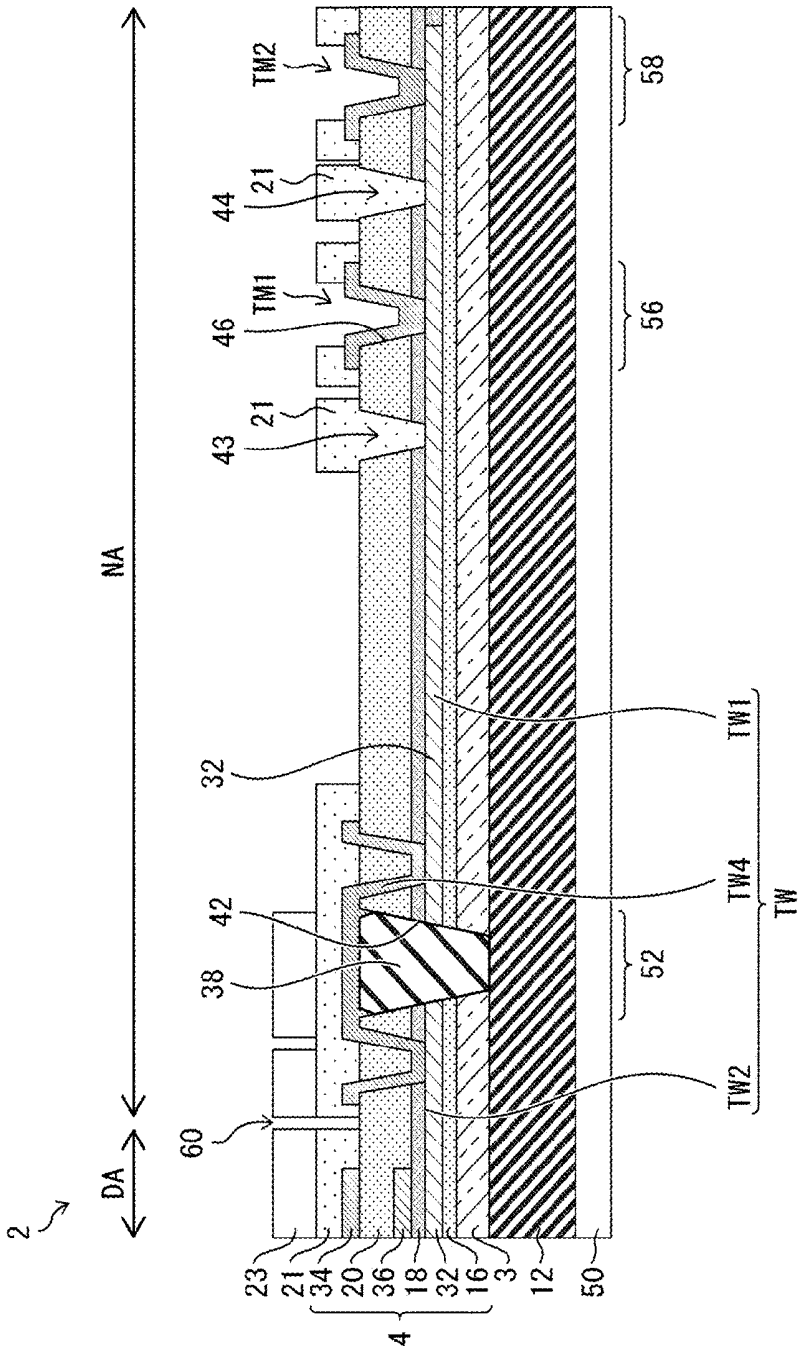
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FIG. 23

DISPLAY DEVICE

TECHNICAL FIELD

[0001] The disclosure is related to a display device.

BACKGROUND ART

[0002] PTL 1 discloses a configuration in which a terminal region is provided outside a display region of an organic EL panel.

CITATION LIST

Patent Literature

[0003] PTL 1: JP 2011-18686 A (publication date: Jan. 27, 2011)

SUMMARY

Technical Problem

[0004] When an IC chip is mounted onto a terminal portion, a crack may occur in the terminal region, and the crack may extend to its surroundings.

Solution to Problem

[0005] A display device according to an aspect of the disclosure includes: a TFT layer including a plurality of inorganic insulating films; and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The display device includes a first slit pattern and a second slit pattern each extending through at least one of the plurality of inorganic insulating films. The first slit pattern is formed between the active region and the terminal region in plan view and also, the terminal region is sandwiched between the first slit pattern and the second slit pattern in plan view.

[0006] A method for manufacturing a display device according to another aspect of the disclosure is a method for manufacturing a display device including a TFT layer including a plurality of inorganic insulating films and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The method including: forming a first slit pattern extending through at least one of the plurality of inorganic insulating films, between the active region and the terminal region in plan view; and forming a second slit pattern extending through at least one of the plurality of inorganic insulating films to sandwich the terminal region together with the first slit pattern in plan view.

[0007] A manufacturing apparatus configured to manufacture a display device according to another aspect of the disclosure is a manufacturing apparatus configured to manufacture a display device including a TFT layer including a plurality of inorganic insulating films and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The manufacturing apparatus is configured to form a first slit pattern extending through at least one of the plurality of inorganic insulating films, between the active region and the terminal region in plan view; and to form a second slit pattern extending through at least one of the plurality of inorganic insulating films to sandwich the terminal region together with the first slit pattern in plan view.

Advantageous Effects of Disclosure

[0008] According to one aspect of the disclosure, even in a case where a crack occurs in a terminal region, a first slit pattern and a second slit pattern prevent the crack from extending to its surroundings.

BRIEF DESCRIPTION OF DRAWINGS

[0009] FIG. **1** is a flowchart illustrating an example of a method for manufacturing an EL device.

[0010] FIG. **2**A is a cross-sectional view illustrating a configuration example of individual EL devices according to several embodiments of the disclosure during formation, and FIG. **2**B is a cross-sectional view illustrating a configuration example of an EL device according to several embodiments of the disclosure.

[0011] FIG. **3**A is a plan view illustrating a configuration example of individual EL devices according to several embodiments of the disclosure, and FIG. **3**B is a partial plan view focusing on a terminal portion of the configuration example illustrated in FIG. **3**A.

[0012] FIG. **4** is a cross-sectional view illustrating a cross-sectional configuration of an EL device before formation of a source conductive layer, according to one embodiment of the disclosure.

[0013] FIG. **5** is a cross-sectional view illustrating a cross-sectional configuration of an EL device after formation of a bank layer, according to the one embodiment of the disclosure.

[0014] FIG. **6** is a cross-sectional view illustrating a cross-sectional configuration of an EL device before formation of a second inorganic insulating film, according to another embodiment of the disclosure.

[0015] FIG. **7** is a cross-sectional view illustrating a cross-sectional configuration of an EL device before formation of a source conductive layer, according to the other embodiment of the disclosure.

[0016] FIG. **8** is a cross-sectional view illustrating a cross-sectional configuration of an EL device after formation of a bank layer, according to the other embodiment of the disclosure.

[0017] FIG. **9** is a cross-sectional view illustrating a cross-sectional configuration of an EL device before formation of a source conductive layer, according to another embodiment of the disclosure.

[0018] FIG. **10** is a cross-sectional view illustrating a cross-sectional configuration of an EL device after formation of a bank layer, according to the other embodiment of the disclosure.

[0019] FIG. **11** is a cross-sectional view illustrating a cross-sectional configuration of an EL device according to another embodiment of the disclosure.

[0020] FIG. **12** is a cross-sectional view illustrating a cross-sectional configuration of an EL device according to another embodiment of the disclosure.

[0021] FIG. **13** is a cross-sectional view illustrating a cross-sectional configuration of an EL device according to another embodiment of the disclosure.

[0022] FIG. **14** is a plan view illustrating a configuration example of individual EL devices according to other embodiments of the disclosure.

[0023] FIG. **15** is a cross-sectional view taken along A-A' line of FIG. **14**, which illustrates a cross-sectional configuration of an EL device according to another embodiment of the disclosure.

[0024] FIG. **16** is another cross-sectional view taken along B-B' line of FIG. **14**, which illustrates a cross-sectional configuration of an EL device according to the other embodiment of the disclosure.

[0025] FIG. **17** is a cross-sectional view taken along A-A' line of FIG. **14**, which illustrates a cross-sectional configuration of an EL device according to another embodiment of the disclosure.

[0026] FIG. **18** is another cross-sectional view taken along B-B' line of FIG. **14**, which illustrates a cross-sectional configuration of an EL device according to the other embodiment of the disclosure.

[0027] FIGS. **19**A to **19**C are plan views or partial enlarged views illustrating several modified examples of a configuration of a slit in each of the EL devices according to the other embodiment of the disclosure.

[0028] FIGS. **20**A and **20**B are plan views illustrating a configuration example of an EL device **2** according to another embodiment of the disclosure.

[0029] FIG. **21** is a cross-sectional view taken along A-A' line of FIG. **20**A, which illustrates a cross-sectional configuration of an EL device according to the other embodiment of the disclosure.

[0030] FIG. **22** is a cross-sectional view taken along B-B' line of FIG. **20**A, which illustrates a cross-sectional configuration of an EL device according to the other embodiment of the disclosure.

[0031] FIG. **23** is a cross-sectional view illustrating a configuration example obtained by combining configurations of EL devices according to several embodiments of the disclosure.

DESCRIPTION OF EMBODIMENTS

[0032] FIG. **1** is a flowchart illustrating an example of a method for manufacturing an EL device. FIG. **2**A is a cross-sectional view illustrating a configuration example of individual EL devices according to several embodiments of the disclosure during formation. FIG. **2**B is a cross-sectional view illustrating a configuration example of individual EL devices according to several embodiments of the disclosure. FIG. **3**A is a plan view illustrating a configuration example of individual EL devices according to several embodiments of the disclosure. FIG. **3**B is a partial plan view focusing on a terminal portion of the configuration example illustrated in FIG. **3**A.

[0033] When a flexible display device is manufactured, as illustrated in FIG. **1** and FIGS. **2**A and **2**B, first, a resin layer **12** is formed on a transparent mother substrate (for example, a glass substrate) **50** (step S**1**). Next, an inorganic barrier film **3** is formed (step S**2**). Next, a TFT layer **4** including a semiconductor film **15**, a plurality of inorganic insulating films **16**, **18**, and **20**, a flattening film **21**, and a plurality of conductive layers **32**, **34**, and **36** are formed (step S**3**). Next, a bank layer **23** and a light emitting element layer (for example, an OLED element layer) **5** are formed (step S**4**). Next, a sealing layer **6** is formed that includes inorganic sealing films **26** and **28** and an organic sealing film **27** (step S**5**). Next, a protection member **9** (a PET film, for example) is bonded to the sealing layer **6**, with an adhesive layer **8** interposed therebetween (step S**6**).

[0034] Next, the resin layer **12** is irradiated with laser light (step S**7**). Here, by the resin layer **12** absorbing the emitted laser light, the lower face of the resin layer **12** (an interface with a mother substrate **50**) changes quality due to ablation, and a peeling layer is formed. This reduces a bonding force between the resin layer **12** and the mother substrate **50**. Next, the mother substrate **50** is peeled from the resin layer **12** (step S**8**). Then, a layered body **7** and the mother substrate **50** illustrated in FIG. **2**A are peeled from each other. Here, the layered body **7** refers to the entire multilayer formed on the mother substrate **50**, that is, in an example illustrated in FIG. **2**A, refers to layers including from the resin layer **12** formed on the mother substrate **50** to a protection member **9**, which is the outermost layer.

[0035] Next, as illustrated in FIG. **2**B, a support member **10** (a PET film, for example) is bonded to the lower face of the resin layer **12**, with an adhesive layer **11** interposed therebetween (step S**9**). Subsequently, the layered body **7** and the support member **10** are separated, and at the same time, the protection member **9** is cut to obtain a plurality of EL devices (step S**10**). Next, the protection member **9** on a terminal portion **51** (see FIG. **3**A) of the TFT layer **4** is peeled off, and terminal exposure is performed (step S**11**). In this way, an EL device **2** illustrated in FIG. **2**B is obtained. After that, a functional film is bonded (step S**12**), and an electronic circuit board is mounted on the terminal portion **51** using an ACF or the like (step S**13**). Note that each of the above steps is performed by an EL device manufacturing apparatus.

[0036] A feature of the EL device manufacturing method according to one embodiment of the disclosure resides particularly in step S**3** and step S**9** above. The details thereof will be described below.

[0037] Examples of the material of the resin layer **12** include polyimide, epoxy, and polyamide. Among these, polyimide is preferably used.

[0038] The inorganic barrier layer **3** is a film configured to prevent water or impurities from reaching the TFT layer **4** or the light emitting element layer **5** when the EL device is being used, and the inorganic barrier layer **3** may be made of a silicon oxide film, silicon nitride film, or silicon oxynitride film formed by CVD, or a layered film thereof, for example. The thickness of the inorganic barrier layer **3** is, for example, from 50 nm to 1500 nm.

[0039] The TFT layer **4** includes a semiconductor film **15**, an inorganic insulating film **16** (a gate insulating film) formed on the semiconductor film **15**, a gate electrode conductive layer **32** formed on the gate insulating film **16**, a first inorganic insulating film **18** formed on the gate electrode conductive layer **32**, an intermediate conductive layer **36** formed on the first inorganic insulating film **18**, a second inorganic insulating film **20** formed on the intermediate conductive layer **36**, a source conductive layer **34** formed on the inorganic insulating film **20**, and a flattening film **21** formed on the conductive layer **34**. In an active region DA of the TFT layer **4**, a gate electrode G is formed from the gate conductive layer **32** for each subpixel, and a source electrode S and a drain electrode D are formed from the source conductive layer **34**. The semiconductor film **15**, the inorganic insulating film **16**, the gate electrode G, the inorganic insulating films **18** and **20**, the source electrode S,

and the drain electrode D constitute a thin film transistor (TFT). In an end portion (non-active region NA) of the TFT layer **4**, formed is the terminal portion **51** including terminals TM and terminal wiring lines TW used for connection with an IC chip and an electronic circuit board such as an FPC. The terminals TM are electrically connected to various wiring lines of the TFT layer **4** through the terminal wiring lines TW. The terminals TM and terminal wiring lines TW are formed from one or more of the plurality of conductive layers **32**, **34**, and **36**.

[0040] The semiconductor film **15** is made of a low-temperature polysilicon (LTPS) or an oxide semiconductor, for example. The gate insulating film **16** can be formed of, for example, a silicon oxide (SiOx) film, a silicon nitride (SiNx) film, or a layered film thereof formed using a CVD method. The gate electrode G, the source electrode S, the drain electrode D, and the terminal are formed of a metal single layer film or a layered film including, for example, at least one of aluminum (Al), tungsten (W), molybdenum (Mo), tantalum (Ta), chromium (Cr), titanium (Ti), or copper (Cu). Note that, in FIGS. **2**A and **2**B, the TFT is illustrated that has a top gate structure in which the semiconductor film **15** functions as the channel, but the TFT may have a bottom gate structure (when the channel of the TFT is formed in the oxide semiconductor, for example).

[0041] The inorganic insulating films **18** and **20** can be constituted by a silicon oxide (SiOx) film or a silicon nitride (SiNx) film, or a layered film of these, formed using CVD. The flattening film **21** is an organic insulating film and can be made of a coatable photosensitive organic material such as polyimide or acrylic, for example.

[0042] The light emitting element layer **5** (an organic light emitting diode layer, for example) includes an anode electrode **22** formed on the flattening film **21**, a partition **23***c* that defines a subpixel of the active region DA, a bank **23***b* formed in the non-active region NA, an electroluminescence (EL) layer **24** formed on the anode electrode **22**, and a cathode electrode **25** formed on the EL layer **24**, and a light emitting element (an organic light emitting diode, for example) is configured by the anode electrode **22**, the EL layer **24**, and the cathode electrode **25**.

[0043] The partition **23***c* and the bank **23***b* may be formed in the bank layer **23** in the same step, for example, using a coatable photosensitive organic material such as polyimide, epoxy, or acrylic. The bank **23***b* of the non-active region NA is formed on the inorganic insulating film **20**. The bank **23***b* defines the edge of the organic sealing film **27**.

[0044] The EL layer **24** is formed by vapor deposition or an ink-jet method in a region (subpixel region) enclosed by the partition **23***c*. In a case that the light emitting element layer **5** is an organic light emitting diode (OLED) layer, for example, the EL layer **24** is formed by layering a hole injecting layer, a hole transport layer, a light emitting layer, an electron transport layer, and an electron injecting layer from the lower layer side.

[0045] The anode electrode **22** is photoreflective and is formed by layering Indium Tin Oxide (ITO) and an alloy containing Ag, for example. The cathode electrode **25** may be made of a transparent metal such as Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO).

[0046] In a case that the light emitting element layer **5** is the OLED layer, positive holes and electrons are recombined inside the EL layer **24** by a drive current between the anode electrode **22** and the cathode electrode **25**, and light is emitted as a result of excitons that are generated by the recombination falling into a ground state.

[0047] The light emitting element layer **5** is not limited to OLED element configurations, and may be an inorganic light emitting diode or a quantum dot light emitting diode.

[0048] The sealing layer **6** includes a first inorganic sealing film **26** configured to cover the partition **23***c* and the cathode electrode **25**, an organic sealing film **27** configured to cover the first inorganic sealing film **26**, and a second inorganic sealing film **28** configured to cover the organic sealing film **27**.

[0049] The first inorganic sealing film **26** and the second inorganic sealing film **28** can be each constituted by a silicon oxide film, a silicon nitride film, or a silicon oxynitride film, or by a layered film of these, formed using CVD. The organic sealing film **27** is a transparent organic insulating film that is thicker than the first inorganic sealing film **26** and the second inorganic sealing film **28**, and may be formed of a coatable photosensitive organic material such as polymide or acrylic. For example, after coating the first inorganic sealing film **26** with an ink containing such an organic material using the ink-jet method, the ink is cured by UV irradiation. The sealing layer **6** covers the light emitting element layer **5** and inhibits foreign matter, such as water and oxygen, from infiltrating to the light emitting element layer **5**.

[0050] Note that the protection member **9** is bonded to the sealing layer **6**, with the adhesive layer **8** interposed therebetween, and functions as a support member when the mother substrate **50** is peeled off. Examples of a material of the protection member **9** include polyethylene terephthalate (PET).

[0051] After the mother substrate **50** has been peeled off, the support member **10** is bonded to the lower face of the resin layer **12** so as to manufacture an EL device having excellent flexibility. Examples of a material of the support member **10** include polyethylene terephthalate (PET). The support member **10** can be selectively removed so as to further provide the EL device **2** with flexibility. For example, a cut-off line is formed in the support member **10** along a target cut-off region before the support member **10** is bonded in step S**9**, and the support member **10** corresponding to the target region is peeled from the EL device **2** in any one of steps S**9** to S**13**, so that the support member **10** can be selectively removed.

[0052] The functional film has an optical compensation function, a touch sensor function, a protective function, and the like, for example. The electronic circuit board is an IC chip or a flexible printed circuit board that is mounted on a plurality of terminals TM, for example.

[0053] As illustrated in FIGS. **3**A and **3**B, the terminal portion **51** includes a bendable region **52** in which the support member **10** is selectively removed, an IC chip mounted region **56** (terminal region) in which terminals TM**1** used for connection with the IC chip are arranged in a staggered manner, and an FPC connection region **58** in which terminals TM**2** used for connection with the FPC are arranged. The IC chip mounted region **56** is located between the active region DA and the FPC connection region **58**, and the bendable region **52** is located between the active region DA and the IC chip mounted region **56**. The EL device **2** can bend along the bendable region **52** so that the active region DA faces upward, and the IC chip mounted region **56** and the FPC connection region **58** face downward. This makes an

effective width of the terminal portion **51** smaller than the entire width and in turn, reduces a frame portion of a display device including the EL device **2**.

[0054] The terminal wiring line TW is led from the active region DA and connected to the terminal TM**1** in the IC chip mounted region **56**.

[0055] A cutout (groove) having certain width and length is referred to as a slit in this specification. Further, one slit, which continuously extends like a solid line, is referred to as a "continuous slit". Regarding a plurality of slits, which are aligned and spaced like a dotted line, each of the slits is referred to as an "island-like slit", and the plurality of slits are referred to as an "aligned slit group". A direction in which the "aligned slit group" extends is a direction in which the "island-like slits" thereof are aligned. For example, a bending slit **42** illustrated in FIG. **3**B and FIG. **19**C is a continuous slit. For example, the bending slit **42** illustrated in FIGS. **19**A and **19**B is an "aligned slit group". Moreover, the slit or slit group, which makes the EL device easily bendable, is referred to as a "bending slit".

First Embodiment

Step S3

[0056] Step S**3**, considered as a feature of one embodiment of the disclosure, will be described.

[0057] In step S**3**, as illustrated in FIGS. **3**A and **3**B, an IC chip outer circumferential slit **40** is formed so as to surround the IC chip mounted region **56** (terminal region). Moreover, the bending slit **42** (third slit pattern) is formed in the bendable region **52** (bending region) through the same process as a process for the IC chip outer circumferential slit **40**.

[0058] The IC chip outer circumferential slit **40** includes a continuous active side slit **43** (first slit pattern) located near the active region DA, a continuous FPC side slit **44** (second slit pattern) located near the FPC connection region **58**, and two continuous end side slits **45** (two slit patterns) located near the end side of the EL device **2**. The active side slit **43** and the FPC side slit **44** extend substantially in parallel to the direction in which the terminal wiring line TW extends. The two end side slits **45** and the bending slit **42** extend substantially orthogonally to the direction in which the terminal wiring line TW extends. In the direction in which the terminal wiring line TW extends, the active region DA, the bendable region **52**, the active side slit **43**, the IC chip mounted region **56**, the FPC side slit **44**, and the FPC connection region **58** are arranged in this order. Note that the IC chip outer circumferential slit **40** can include only the active side slit **43** and the FPC side slit **44**, not including the end side slit **45**.

[0059] FIG. **4** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the first embodiment before formation of the source conductive layer **34**. FIG. **5** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the first embodiment after formation of the bank layer **23**.

[0060] As illustrated in FIGS. **4** and **5**, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** similarly extend through the second inorganic insulating film **20** and reach the first inorganic insulating film **18**. Although not illustrated in FIGS. **4** and **5**, the end side slits **45** similarly extend through the second inorganic insulating film **20** and reach the first inorganic insulating film **18**.

[0061] The terminal wiring line TW is made from the gate conductive layer **32** alone. The terminal wiring line TW extends above the resin layer **12** and below the bending slit **42**, the active side slit **43**, and the FPC side slit **44** (hereinafter collectively referred to as "slits **42** to **44**"), crossing the bending slit **42** and the active side slit **43**.

[0062] As illustrated in FIG. **5**, the terminals TM**1** and TM**2** (i) similarly are in contact with the terminal wiring line TW through a contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0063] The slits **42** to **44**, the terminal wiring line TW, and the terminals TM**1** and TM**2** of FIGS. **4** and **5** can be formed in step **3** through the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0064] First, the semiconductor film **15** and the gate insulating film **16** are formed. Next, the gate conductive layer **32** is formed, and the terminal wiring line TW as well as the gate electrode G are made from the gate conductive layer **32**. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Next, the first inorganic insulating film **18** and the second inorganic insulating film **20** are etched so as to form the contact hole **46** for the terminals TM**1** and TM**2**. Subsequently, the source conductive layer **34** is formed, and the terminals TM**1** and TM**2** as well as the source electrode S and the drain electrode D are made from the source conductive layer **34**. Next, the first inorganic insulating film **18** and the second inorganic insulating film **20** are etched again so as to form the slits **42** to **44**. Subsequently, the flattening film **21** is formed.

[0065] Note that the etching for forming the slits **42** to **44** can be performed at a timing between the formation of the second inorganic insulating film **20** and the formation of the contact hole **46**, at a timing between the formation of the contact hole **46** and the formation of the source conductive layer **34**, or at the same timing as the etching for forming the contact hole **46**. Here, in the latter case, the slits **42** to **44** are formed through etching with the same mask as a mask for the contact hole **46**, and the gate conductive layer **32** is exposed at the bottom surface of the slits **42** to **44**. Thus, in that latter case, the exposed gate conductive layer **32** can be covered by filling the slits **42** to **44** with the flattening film **21** or other such insulating material.

[0066] Accordingly, to prevent shortcircuiting of the terminal wiring line TW, it is preferred to perform the etching for forming the slits **42** to **44** at a timing between the formation of the source conductive layer **34** and the formation of the flattening film **21**.

[0067] Further, the gate conductive layer **32** preferably functions as an etching stop layer.

Bank Layer

[0068] As illustrated in FIG. **5**, the bank layer **23** obtained in step **4** is preferably formed on the bending slit **42** so as to reinforce the bendable region **52** of the EL device **2**. This is because the bendable region **52** having the bending slit **42** receives a mechanical stress. On the other hand, the bank layer **23** is preferably not formed on the IC chip outer circumferential slit **40** (including the slits **43** and **44**). This

is because the IC chip outer circumferential slit **40** is located around the IC chip mounted region **56**, so that when the bank layer **23** is formed on the IC chip outer circumferential slit **40**, the IC chip cannot be easily connected to the terminal TM1.

[0069] The slit **60** is preferably formed extending through the flattening film **21** and the bank layer **23**, at or around the boundary between the active region DA and the non-active region NA in step **4** or its subsequent steps. This is because the flattening film **21** and the bank layer **23** are organic insulating films; when the slit **60** is not formed, water that has permeated to the flattening film **21** and the bank layer **23** may possibly reach the active region DA from the non-active region NA.

Step S9

[0070] Step S9 above, considered as a feature of one embodiment of the disclosure, will be described hereinafter.

[0071] Although not illustrated, the support member **10** is selectively removed from the bendable region **52** in step S9 so that the EL device **2** can have flexibility at the bendable region **52**. Alternatively, the support member **19** is not selectively bonded to the bendable region **52**.

Advantageous Effects

[0072] The support member **10** is not bonded to the bendable region **52**, and the bending slit **42** reaches the first inorganic insulating film **18** extending through the second inorganic insulating film **20** as illustrated in FIGS. **4** and **5**. Thus, the EL device **2** becomes flexible and bendable at the bendable region **52** compared with the non-active region NA other than the bendable region **52**.

[0073] As illustrated in FIGS. **4** and **5**, the terminal wiring line TW passes below the bending slit **42** and the active side slit **43**, crossing the bending slit **42** and the active side slit **43**. Thus, the bending slit **42** and the active side slit **43** can be each formed as a single continuous slit. This facilitates the formation thereof.

[0074] As illustrated in FIGS. **4** and **5**, the IC chip outer circumferential slit **40** surrounding the IC chip mounted region **56** reaches the first inorganic insulating film **18** extending through the second inorganic insulating film **20**. Thus, even when a strong pressure is applied when mounting the IC chip, for example, and then, a crack occurs in at least one of the first inorganic insulating film **18** and the second inorganic insulating film **20** of the IC chip mounted region **56**, the crack does not extend over the IC chip outer circumferential slit **40** and thus is less likely to disconnect the terminal wiring line TW, whereby the EL device **2** maintains its reliability.

Second Embodiment

[0075] Step S3, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIGS. **6** to **8**. Note that step S9, considered as a feature of the present embodiment, is the same as step S9 by which the first embodiment is characterized, and therefore, its description is omitted here.

[0076] FIG. **6** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the second embodiment before the formation of the second inorganic insulating film **20**. FIG. **7** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the second embodiment before the formation of the source conductive layer **34**. FIG. **8** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the second embodiment after formation of the bank layer **23**.

[0077] As illustrated in FIGS. **6** to **8**, the bending slit **42** includes a continuous lower bending slit **42***a* extending through the inorganic barrier film **3**, the gate insulating film **16**, and the first inorganic insulating film **18**, and a continuous upper bending slit **42***b* extending through the second inorganic insulating film **20**. The active side slit **43** similarly includes a continuous lower active side slit **43***a* extending through the inorganic barrier film **3**, the gate insulating film **16**, and the first inorganic insulating film **18**, and a continuous upper active side slit **43***b* extending through the second inorganic insulating film **20**. The FPC side slit **44** similarly includes a continuous lower FPC side slit **44***a* extending through the inorganic barrier film **3**, the gate insulating film **16**, and the first inorganic insulating film **18**, and a continuous upper FPC side slit **44***b* extending through the second inorganic insulating film **20**. Although not illustrated in FIGS. **6** to **8**, the two end side slits **45** each include a continuous lower end side slit extending through the inorganic barrier film **3**, the gate insulating film **16**, and the first inorganic insulating film **18** and a continuous upper end side slit extending through the second inorganic insulating film **20**.

[0078] The terminal wiring line TW includes a main body portion TW**1**, an active side portion TW**2**, and a terminal side portion TW**3**, which are made from the gate conductive layer **32**, and a bending slit bridge portion TW**4** and an outer circumferential slit bridge portion TW**5**, which are made from the intermediate conductive layer **36**. The bridge portions TW**4** and TW**5** of the terminal wiring line TW pass inner surfaces and bottom surfaces of the lower bending slit **42***a* and the lower active side slit **43***a*, crossing the bending slit **42** and the active side slit **43**. To prevent the bridge portions TW**4** and TW**5** of the terminal wiring line TW from being exposed, the flattening film **21** is formed on the bridge portions TW**4** and TW**5** of the terminal wiring line TW.

[0079] As illustrated in FIG. **8**, the terminals TM**1** and TM**2** (i) similarly are in contact with the terminal side portion TW**3** of the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0080] The terminal wiring line TW, the slits **42** to **44**, and the terminals TM**1** and TM**2** illustrated in FIGS. **6** to **8** can be formed in step **3** in accordance with the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0081] First, the semiconductor film **15** and the gate insulating film **16** are formed. Subsequently, the gate conductive layer **32** is formed, and the main body portion TW**1**, the active side portion TW**2**, and the terminal side portion TW**3** of the terminal wiring line TW as well as the gate electrode G are made from the gate conductive layer **32**. Next, the first inorganic insulating film **18** is formed. Then, the inorganic barrier film **3**, the gate insulating film **16**, and the first inorganic insulating film **18** are etched so as to form the lower bending slit **42***a*, the lower active side slit **43***a*, and the lower FPC side slit **44***a* and contact holes for connection

between the main body portion TW1, the active side portion TW2, and the terminal side portion TW3 of the terminal wiring line TW and the bridge portions TW4 and TW5. Next, the intermediate conductive layer **36** is formed, and the bridge portions TW4 and TW5 of the terminal wiring line TW are made from the intermediate conductive layer **36**. Then, the second inorganic insulating film **20** is formed. Next, the second inorganic insulating film **20** is etched so as to form the contact hole **46** for the terminals TM1 and TM2. After that, the source conductive layer **34** is formed, and the terminals TM1 and TM2 as well as the source electrode S and the drain electrode D are made from the source conductive layer **34**. Next, the second inorganic insulating film **20** is etched again to form the upper bending slit **42***b*, the upper active side slit **43***b*, and the upper FPC side slit **44***b*. Subsequently, the flattening film **21** is formed.

[0082] Note that the etching for forming the upper bending slit **42***b*, the upper active side slit **43***b*, and the upper FPC side slit **44***b* can be performed, similar to the etching for forming the slits **42** to **44** in the first embodiment above, at a timing between the formation of the second inorganic insulating film **20** and the formation of the contact hole **46** or at a timing between the formation of the contact hole **46** and the formation of the source conductive layer **34**, or otherwise at the same timing as the etching for forming the contact hole **46**. In this last case, the exposed gate conductive layer **32** can be covered by filling the slits **42** to **44** with the flattening film **21** or other such insulating material.

[0083] Moreover, the gate conductive layer **32** and the intermediate conductive layer **36** preferably function as an etching stop layer. To prevent disconnection of the bridge portions TW4 and TW5 of the terminal wiring line TW, the lower bending slit **42***a* and the lower active side slit **43***a* are preferably tapered, i.e., reduce their width toward the bottom, and more preferably tapered with a small angle. Further, the etching of the plurality of inorganic insulating layer can be performed in a plurality of steps instead of the single step.

Advantageous Effects

[0084] The support member **10** is not bonded to the bendable region **52**, and the bending slit **42** extends through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** as illustrated in FIGS. **6** to **8**. Thus, the EL device **2** becomes flexible and bendable at the bendable region **52** compared with the non-active region NA other than the bendable region **52**. Further, the EL device **2** having a configuration illustrated in FIG. **8** is more bendable than the EL device **2** having a configuration illustrated in FIG. **5**.

[0085] As illustrated in FIGS. **7** and **8**, the bridge portions TW4 and TW5 of the terminal wiring line TW pass the inner surfaces and bottom surfaces of the lower bending slit **42***a* and the lower active side slit **43***a*, crossing the bending slit **42** and the active side slit **43**. Thus, the bending slit **42** and the active side slit **43** can be each formed as a single continuous slit. This facilitates the formation thereof.

[0086] As illustrated in FIGS. **6** to **8**, the IC chip outer circumferential slit **40** surrounding the IC chip mounted region **56** extends through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Therefore, even when a large pressure is applied when mounting an IC chip, for example, and then, a crack occurs in at least one of the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** of the IC chip mounted region **56**, the crack does not extend over the IC chip outer circumferential slit **40** and thus is not less likely to disconnect the terminal wiring line TW, whereby the EL device **2** maintains its reliability. Further, the EL device **2** having a configuration illustrated in FIG. **8** maintains a higher reliability than the EL device **2** having a configuration illustrated in FIG. **5**.

Third Embodiment

[0087] Step S3, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIGS. **9** and **10**. Note that step S9, considered as a feature of the present embodiment, is the same as step S9 by which the second embodiment is characterized, and therefore, its description is omitted here.

[0088] FIG. **9** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the third embodiment before formation of the source conductive layer **34**. FIG. **10** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the third embodiment after formation of the bank layer **23**.

[0089] As illustrated in FIGS. **9** and **10**, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Although not illustrated in FIGS. **9** and **10**, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0090] The terminal wiring line TW includes the main body portion TW1, the active side portion TW2, and the terminal side portion TW3, which are made from the gate conductive layer **32**, and the bending slit bridge portion TW4 and the outer circumferential slit bridge portion TW5 made from the source conductive layer **34**. The bridge portions TW4 and TW5 of the terminal wiring line TW each pass the inner surfaces and bottom surfaces of the bending slit **42** and the active side slit **43**, crossing the bending slit **42** and the active side slit **43**. To prevent the respective bridge portions TW4 and TW5 of the terminal wiring line TW from being exposed, the flattening film **21** is formed on the bridge portions TW4 and TW5 of the terminal wiring line TW.

[0091] As illustrated in FIG. **10**, the terminals TM1 and TM2 (i) similarly are in contact with the terminal side portion TW3 of the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0092] The terminal wiring line TW, the slits **42** to **44**, and the terminals TM1 and TM2 illustrated in FIGS. **9** and **10** can be formed in step **3** in accordance with the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0093] First, the semiconductor film **15** and the gate insulating film **16** are formed. Next, the gate conductive layer **32** is formed, and the main body portion TW1, the active side

portion TW2, and the terminal side portion TW3 of the terminal wiring line TW as well as the gate electrode G are made from the gate conductive layer **32**. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Next, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched so as to form the bending slit **42**, the active side slit **43**, and the FPC side slit **44**, and contact holes for connection between the main body portion TW1, the active side portion TW2, and the terminal side portion TW3 of the terminal wiring line TW and the bridge portions TW4 and TW5 as well as the contact hole **46** for the terminals TM1 and TM2. Subsequently, the source conductive layer **34** is formed, and the terminals TM1 and TM2 and the bridge portions TW4 and TW5 of the terminal wiring line TW as well as the source electrode S and the drain electrode D are made from the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0094] Moreover, the gate conductive layer **32** and the intermediate conductive layer **36** preferably function as an etching stop layer. Further, to prevent disconnection of the bridge portions TW4 and TW5 of the terminal wiring line TW, the bending slit **42** and the active side slit **43** are preferably tapered, i.e., reduces its width toward the bottom, and more preferably, has a small taper angle at the inner surface.

Advantageous Effects

[0095] The EL device **2** having a configuration illustrated in FIG. **10** can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **7**.

[0096] Moreover, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** can be formed together with the contact hole **46** for the terminals TM1 and TM2. Thus, it is possible to reduce the number of steps in a method for manufacturing the EL device **2** having a configuration illustrated in FIG. **10** compared with that for the EL device **2** illustrated in FIG. **7**.

Fourth Embodiment

[0097] Step S3, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIG. **11**. Note that step S9, considered as a feature of the present embodiment, is the same as step S9 by which the second embodiment is characterized, and therefore, its description is omitted here.

[0098] FIG. **11** is a cross-sectional view illustrating a cross-sectional configuration of an EL device **2** according to the fourth embodiment.

[0099] As illustrated in FIG. **11**, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Moreover, although a description is omitted, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0100] The terminal wiring line TW includes the main body portion TW1, the active side portion TW2, and the terminal side portion TW3, which are made from the gate conductive layer **32**, and the bending slit bridge portion TW4 and the outer circumferential slit bridge portion TW5 made from the source conductive layer **34**. The bridge portions TW4 and TW5 of the terminal wiring line TW pass above the bending slit **42** and the active side slit **43** and specifically, pass above a buried material **38** filled into the bending slit **42** and the active side slit **43**, crossing the bending slit **42** and the active side slit **43**.

[0101] The buried material **38**, which is an organic insulating material, can be made from, for example, a coatable photosensitive organic material such as polyimide and acrylic. The buried material **38** can be made from the same material as or different material from the flattening film **21**.

[0102] The terminals TM1 and TM2 (i) similarly are in contact with the terminal side portion TW3 of the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0103] The terminal wiring line TW and the slits **42** to **44** illustrated in FIG. **11** can be formed in step S3 in accordance with the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0104] First, the semiconductor film **15** and the gate insulating film **16** are formed. Next, the gate conductive layer **32** is formed, and the main body portion TW1, the active side portion TW2, and the terminal side portion TW3 of the terminal wiring line TW as well as the gate electrode G are made from the gate conductive layer **32**. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Next, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched so as to form the contact hole **46** for the terminals TM1 and TM2, the slits **42** to **44**, and the contact holes for connection between the bridge portions TW4 and TW5 and the main body portion TW1, the active side portion TW2, and the terminal side portion TW3 of the terminal wiring line TW. Subsequently, the insides of the bending slit **42** and the active side slit **43** are filled with the buried material **38**. Subsequently, the source conductive layer **34** is formed, the terminals TM1 and TM2 and the bridge portions TW4 and TW5 of the terminal wiring line TW as well as the source electrode S and the drain electrode D are made from the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0105] The gate conductive layer **32** and the intermediate conductive layer **36** preferably function as an etching stop layer. The insides of the FPC side slit **44** and the two end side slits **45** may be filled with the buried material **38**.

Advantageous Effects

[0106] The EL device **2** having a configuration illustrated in FIG. **11** can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **9**.

[0107] Moreover, according to the configuration illustrated in FIG. **11**, the bridge portions TW4 and TW5 of the terminal wiring line TW pass over the buried material **38** with which the bending slit **42** and the active side slit **43** are filled instead of passing the inner surfaces and the bottom surfaces of the bending slit **42** and the active side slit **43**.

Hence, even in a case where the bending slit **42** and the active side slit **43** have a steep taper angle at their inner surfaces or the bending slit **42** and the active side slit **43** have a large depth, the bridge portions TW**4** and TW**5** of the terminal wiring line TW are hardly disconnected.

Fifth Embodiment

[0108] Step S**3**, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIG. **12**. Note that step S**9**, considered as a feature of the present embodiment, is the same as step S**9** by which the second embodiment is characterized, and therefore, its description is omitted here.

[0109] FIG. **12** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the fifth embodiment.

[0110] As illustrated in FIG. **12**, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Although not illustrated in FIG. **12**, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0111] The terminal wiring line TW includes the terminal side portion TW**3** formed from the gate conductive layer **32** and the main body portion TW**1** formed from only the source conductive layer **34**. The terminal side portion TW**3** of the terminal wiring line TW is provided between the active side slit **43** and the FPC side slit **44**, passing below the second inorganic film **20**. Thus, the terminal TM**1** can come into contact with the terminal wiring line TW inside the TFT layer **4**. This prevents the terminal wiring line TW from being exposed in a region having no flattening film **21**. The main body portion TW**1** of the terminal wiring line TW passes the inner surfaces and the bottom surfaces of the bending slit **42** and the active side slit **43**, crossing the bending slit **42** and the active side slit **43**.

[0112] The terminals TM**1** and TM**2** (i) similarly are in contact with the terminal side portion TW**3** of the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0113] The terminal wiring line TW and the slits **42** to **44** of FIG. **12** can be formed in step **3** through the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0114] First, the semiconductor film **15** and the gate insulating film **16** are formed. Subsequently, the gate conductive layer **32** is formed, and the terminal side portion TW**3** of the terminal wiring line TW as well as the gate electrode G are formed from the gate conductive layer **32**. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Subsequently, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched so as to form the contact hole **46** for the terminals TM**1** and TM**2**, the slits **42** to **44**, and contact holes for connection between the terminal side portion TW**3** of the terminal wiring line TW and the main body portion TW**1**. After that, the source conductive layer **34** is formed, and the terminals TM**1** and TM**2** and the main body portion TW**1** of the terminal wiring line TW as well as the source electrode S and the drain electrode D are formed from the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0115] Further, the gate conductive layer **32** preferably functions as an etching stop layer. Further, to prevent the disconnection of the main body portion TW**1** of the terminal wiring line TW, the bending slit **42** and the active side slit **43** preferably have a tapered shape, i.e., reduce their widths toward the bottom, more preferably have a small taper angle at their inner surfaces.

Advantageous Effects

[0116] The EL device **2** having a configuration illustrated in FIG. **12** can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **10**.

[0117] Moreover, in the EL device **2** illustrated in FIG. **12**, the main body portion TW**1** of the terminal wiring line TW (especially, a portion between the active region DA and the active side slit **43**) is formed from the source conductive layer **34** having a lower resistance than that of the gate conductive layer **32**. Thus, the EL device **2** having a configuration illustrated in FIG. **12** allows a delay in data signal to reduce and in turn, ensures a large margin for design compared with the EL device **2** having a configuration illustrated in FIG. **10**.

Sixth Embodiment

[0118] Step S**3**, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIG. **13**. Note that step S**9**, considered as a feature of the present embodiment, is the same as step S**9** by which the second embodiment is characterized, and therefore, its description is omitted here.

[0119] FIG. **13** is a cross-sectional view illustrating a cross-sectional configuration of the EL device **2** according to the sixth embodiment.

[0120] As illustrated in FIG. **13**, the bending slit **42**, the active side slit **43**, and the FPC side slit **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Moreover, although not illustrated in FIG. **13**, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0121] The terminal wiring line TW includes the terminal side portion TW**3** formed from the gate conductive layer **32** and the main body portion TW**1** formed from only the source conductive layer **34**. Since the terminal side portion TW**3** of the terminal wiring line TW passes below the second inorganic film **20**, the terminal wiring line TW is not exposed at a region having no flattening film **21**. The main body portion TW**1** of the terminal wiring line TW passes the inner surfaces and the bottom surfaces of the bending slit **42** and the active side slit **43**, crossing the bending slit **42** and the active side slit **43**.

[0122] The terminals TM**1** and TM**2** (i) similarly are in contact with the terminal side portion TW**3** of the terminal

wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0123] The terminal wiring line TW and the slits **42** to **44** of FIG. **13** can be formed in step **3** through the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the active side slit **43** and the FPC side slit **44**.

[0124] First, the semiconductor film **15** and the gate insulating film **16** are formed. Subsequently, the gate conductive layer **32** is formed, and the terminal side portion TW**3** of the terminal wiring line TW as well as the gate electrode G are formed from the gate conductive layer **32**. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Subsequently, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched so as to form the contact hole **46** for the terminal TM, the slits **42** to **44**, and contact holes for connection between the terminal side portion TW**3** of the terminal wiring line TW and the main body portion TW**1**. Subsequently, the insides of the bending slit **42** and the active side slit **43** are filled with the buried material **38**. After that, the source conductive layer **34** is formed, and the terminals TM**1** and TM**2** and the main body portion TW**1** of the terminal wiring line TW as well as the source electrode S and the drain electrode D are formed from the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0125] The gate conductive layer **32** preferably functions as an etching stop layer. The insides of the FPC side slit **44** and the two end side slits **45** may be filled with the buried material **38**.

Advantageous Effects

[0126] The EL device **2** having a configuration illustrated in FIG. **13** can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **11**.

[0127] Moreover, in the EL device **2** having a configuration illustrated in FIG. **13**, the main body portion TW**1** of the terminal wiring line TW (especially, a portion between the active region DA and the active side slit **43**) is formed from the source conductive layer **34** having a lower resistance than that of the gate conductive layer **32**. Thus, the EL device **2** having a configuration illustrated in FIG. **13** allows a delay in data signal to reduce and in turn, ensures a large margin for design compared with the EL device **2** having a configuration illustrated in FIG. **11**.

Seventh Embodiment

[0128] Step S**3**, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIGS. **14** to **16**. Note that step S**9**, considered as a feature of the present embodiment, is the same as step S**9** by which the second embodiment is characterized, and therefore, its description is omitted here.

[0129] FIG. **14** is a plan view illustrating a configuration example of the EL device **2** according to the seventh embodiment or the subsequent eighth embodiment.

[0130] As illustrated in FIG. **14**, the active side slit **43** included in the IC chip outer circumferential slit **40** can include a plurality of island-like slits **43'** instead of one continuous slit. For example, it can be one aligned slit group including the island-like slits **43'** aligned in a direction crossing the direction in which the terminal wiring line TW extends. The bending slit **42** can similarly include a plurality of island-like slits **42'** instead of one continuous slit. That is, it can be one aligned slit group including the island-like slits **42'** aligned in a direction crossing the direction in which the terminal wiring line TW extends. The island-like slits **42'** and **43'** preferably have the length in the direction crossing the terminal wiring line TW, which is shorter than twice the wiring pitch of the terminal wiring line TW and also longer than the wiring pitch of the terminal wiring line TW.

[0131] The terminal wiring line TW extends not to overlap (i.e., cross) the bending slit **42** and the active side slit **43** in plan view. Thus, the terminal wiring line TW passes between the island-like slits **42'** included in the bending slit **42** and the island-like slits **43'** included in the active side slit **43** in plan view. Regarding one aligned slit group included in the bending slit **42**, it is preferable that (i) the individual terminal wiring lines TW pass between different pairs of island slits **42'** and (ii) the total distance of gaps between the island-like slits **42'** be small. Hence, a plurality of island-like slits **42'** constituting one aligned slit group included in the bending slit **42** are preferably arranged such that the individual terminal wiring lines TW pass between the different pairs of island-like slits **42'** in a one-to-one correspondence. Likewise, a plurality of island-like slits **43'** constituting one aligned slit group included in the active side slit **43** are preferably arranged such that the individual terminal wiring lines TW pass between different pairs of island-like slits **43'** in a one-to-one correspondence.

[0132] FIG. **15** is a cross-sectional view taken along A-A' line of FIG. **14**, which illustrates a cross-sectional configuration of the EL device **2** according to the seventh embodiment. FIG. **16** is a cross-sectional view taken along B-B' line of FIG. **14**, which illustrates a cross-sectional configuration of the EL device **2** according to the seventh embodiment. The A-A' section of FIG. **14** is obtained so as not to include the terminal wiring line TW and so as to include the bending slit **42** and the active side slit **43**. Moreover, the B-B' section of FIG. **14** is obtained so as to include the terminal wiring line TW and so as not to include the bending slit **42** and the active side surrounding slit **43**.

[0133] As illustrated in FIG. **15**, the bending slit **42'**, the active side slit **43'**, and the FPC side slit **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Although not illustrated in FIG. **15**, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0134] As illustrated in FIG. **16**, the terminal wiring line TW is formed from only the gate conductive layer **32**. The terminal wiring line TW passes between the island-like slits **42'** included in the bending slit **42** and between the island-like slits **43'** included in the active side slit **43**.

[0135] The terminals TM**1** and TM**2** (i) similarly are in contact with the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0136] The terminal wiring line TW, the island-like slits **42'** and **43'**, and the FPC side slit **44** (hereinafter collectively referred to as "slits **42'**, **43'**, and **44**) of FIGS. **14** to **16** can be formed in step **3** through the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the island-like slit **43'** included in the active side slit **43** and the FPC side slit **44**.

[0137] First, the semiconductor film **15**, the gate insulating film **16**, the gate conductive layer **32**, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Next, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched to form the slits **42'**, **43'**, and **44** as well as the contact hole **46** for the terminals TM1 and TM2. After that, the source conductive layer **34** is formed, and the terminals TM1 and TM2 and the terminal wiring line TW as well as the source electrode S and the drain electrode D are formed form the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0138] The gate conductive layer **32** preferably functions as an etching stop layer. Further, the slits **42'**, **43'**, and **44** can be each formed, similar to the second embodiment, through two-step etching, one for a lower bending slit **42'**a, a lower active side slit **43'**a, and a lower FPC side slit **44**a and the other for an upper bending slit **42'**b, an upper active side slit **43'**b, and an upper FPC side slit **44***b*.

Advantageous Effects

[0139] As illustrated in FIGS. **15** and **16**, the support member **10** is not bonded to the bendable region **52**, and the bending slit **42** extends through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Thus, the EL device **2** becomes flexible and bendable at the bendable region **52** compared with the non-active region NA other than the bendable region **52**. Also, the EL device **2** according to the seventh embodiment is bendable than the EL device **2** having a configuration according to the first embodiment.

[0140] As illustrated in FIG. **15**, the IC chip outer circumferential slit **40** surrounding the IC chip mounted region **56** extends through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Hence, even in a case where a crack occurs in any one or more of the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** of the IC chip mounted region **56**, the crack does not extend over the IC chip outer circumferential slit **40** and thus is less likely to disconnect the terminal wiring line TW, whereby the EL device **2** maintains its reliability. Also, the EL device **2** according to the seventh embodiment maintains higher reliability than the EL device **2** having a configuration according to the first embodiment.

[0141] As illustrated in FIGS. **14** and **16**, the terminal wiring lines TW pass between the island-like slits **42'** included in the bending slit **42** and the island-like slits **43'** included in the active side slit **43**. Therefore, even in a case where the island-like slits **42'** and **43'** included in the bending slit **42** and the active side slit **43** have a sharp taper angle at their inner surfaces or have a large depth, the terminal wiring line TW is hardly disconnected.

[0142] Accordingly, the EL device **2** having a configuration according to the seventh embodiment can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **9**.

Modified Embodiment

[0143] FIGS. **19**A to **19**C are plan views illustrating several modified embodiments of the bending slit **42** and the IC chip outer circumferential slit **40** according to the seventh embodiment or the subsequent eighth embodiment.

[0144] As illustrated in FIGS. **19**A and **19**B, the bending slit **42** and the active side slit **43** can include a plurality of aligned slit groups. Also, the island-like slits **42'** and **43'** included in the plurality of aligned slit groups are arranged in a staggered manner. Specifically, the island-like slits **42'** and **43'** each included in the same aligned slit group are aligned in a direction crossing the direction in which the terminal wiring line TW extends. Different aligned slit group is adjacent to the above aligned slit group in the direction in which the terminal wiring TW extends such that the island-like slits **42'** and **43'** each included in one aligned slit group and the island-like slits **42'** and **43'** included in different aligned slit group are disposed alternately. As a result, the island-like slits **42'** and **43'** included in the plurality of aligned slit groups are arranged in a staggered manner. The staggered arrangement is one kind of alternate arrangement. Moreover, the island-like slits **42'** and **43'** included in the plurality of aligned slit groups are arranged such that a gap between the island-like slits **42'** included in a certain aligned slit group and a gap between the island-like slits **43'** of a certain aligned slit group out of the plurality of aligned slit groups are blocked by the island-like slits **42'** included in another aligned slit group and the island-like slits **43'** included in another aligned slit group, respectively, as viewed in the direction in which the terminal wiring line TW extends. Preferably, the island-like slits **42'** and **43'** included in the plurality of aligned slit groups are arranged such that ends of island-like slits **42'** and **43'** of a certain aligned slit group out of the plurality of aligned slit groups overlap with those of island-like slits **42'** and **43'** of another aligned slit group thereof as viewed in the direction in which the terminal wiring line TW extends.

[0145] The terminal wiring lines TW circumvent the plurality of staggered island-like slits **42'** and **43'** so as not to pass into the island-like slits **42'** and **43'** in plan view. Preferably, the plurality of staggered island-like slits **42'** and **43'** are disposed such that the individual terminal wiring lines TW pass between a corresponding pair of island-like slits **42'** and **43'** constituting each aligned slit group in a one-to-one correspondence.

[0146] The bending slit **42** including a plurality of aligned slit groups makes the EL device **2** more flexible than that including a single aligned slit group. Thus, the EL device **2** more easily bends at the bendable region **52**.

[0147] The active side slit **43** including a plurality of aligned slit groups allows the EL device **2** to maintain its reliability compared with a case that the active side slit **43** includes a single aligned slit group. This is because even when a crack occurs in any one or more of the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** of the IC chip mounted region **56** and spreads through

between the island-like slits **43'** included the inner aligned slit group, the outer aligned slit group can block the spreading of the crack.

[0148] Alternatively, as illustrated in FIG. **19**C, the bending slit **42** being a single continuous slit and the active side slit **43** including one or more aligned slit groups can be combined. In this case, the terminal wiring lines TW crossing the bending slit **42** can have a configuration similar to a configuration described in any of the first embodiment (see FIGS. **4** and **5**), the second embodiment (see FIGS. **6** to **8**), the third embodiment(see FIGS. **9** and **10**), and the fourth embodiment (see FIG. **11**).

[0149] The bending slit **42** being a single continuous slit can make the EL device **2** more flexible than that being a single aligned slit group. Thus, the EL device **2** more easily bends at the bendable region **52**. Further, the bending slit **42** being a single continuous slit can be formed in a narrower bendable region **42** than that including a plurality of aligned slit groups. Therefore, an effective width of the terminal portion **51** can be reduced.

Eighth Embodiment

[0150] Step S**3**, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIGS. **14**, **17**, and **18**. Note that step S**9**, considered as a feature of the present embodiment, is the same as step S**9** by which the second embodiment is characterized, and therefore, its description is omitted here.

[0151] FIG. **17** is a cross-sectional view taken along A-A' line of FIG. **14**, which illustrates a cross-sectional configuration of the EL device **2** according to the eighth embodiment. FIG. **18** is another cross-sectional view taken along B-B' line of FIG. **14**, which illustrates a cross-sectional configuration of the EL device **2** according to the eighth embodiment.

[0152] As illustrated in FIG. **17**, slits **42'**, **43'**, and **44** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**. Although not illustrated in FIG. **17**, the two end side slits **45** similarly extend through the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20**.

[0153] As illustrated in FIG. **18**, the terminal wiring line TW includes the terminal side portion TW**3** formed from the gate conductive layer **32** and the main body portion TW**1** formed from only the source conductive layer **34**. The terminal side portion TW**3** of the terminal wiring line TW is provided in the IC chip mounted region **56** and the FPC connection region **58** and passes below the second inorganic film **20**. Thus, the terminal TM**1** can come into contact with the terminal wiring line TW inside the TFT layer **4**. This prevents the terminal wiring line TW from being exposed in a region having no flattening film **21**. The main body portion TW**1** of each of the terminal wiring lines TW passes a gap between the island-like slits **42'** included in the bending slit **42** and a gap between the island-like slits **43'** included in the active side slit **43**. Therefore, even in a case where the island-like slits **42'** and **43'** included in the bending slit **42** and the active side slit **43** have a sharp taper angle at their inner surfaces or have a large depth, the terminal wiring line TW is hardly disconnected.

[0154] The terminals TM**1** and TM**2** (i) similarly are in contact with the terminal side portion TW**3** of the terminal wiring line TW through the contact hole **46** and (ii) each have an end covered with the flattening film **21** or the bank layer **23**.

Step Sequence

[0155] The terminal wiring line TW and the slits **42'**, **43'**, and **44** of FIGS. **14**, **17**, and **18** can be formed in step **3** through the following step sequence. Note that although a description is omitted, the two end side slits **45** are formed through the same process as a process for the island-like slit **43'** included in the active side slit **43** and the FPC side slit **44**.

[0156] First, the semiconductor film **15** and the gate insulating film **16** are formed. Next, the gate conductive layer **32** is formed, and the terminal side portion TW**3** of the terminal wiring line TW as well as the gate electrode are formed from the gate conductive layer. Subsequently, the first inorganic insulating film **18**, the intermediate conductive layer **36**, and the second inorganic insulating film **20** are formed. Next, the inorganic barrier film **3**, the gate insulating film **16**, the first inorganic insulating film **18**, and the second inorganic insulating film **20** are etched so as to form the contact hole **46** for the terminals TM**1** and TM**2**, the slits **42'**, **43'**, and **44**, and contact hole for connection between the terminal side portion TW**3** of the terminal wiring line TW and the main body portion TW**1**. After that, the source conductive layer **34** is formed, and the terminals TM**1** and TM**2** and the main body portion TW**1** of the terminal wiring line TW as well as the source electrode S and the drain electrode D are formed from the source conductive layer **34**. Subsequently, the flattening film **21** is formed.

[0157] The gate conductive layer **32** preferably functions as an etching stop layer.

Advantageous Effects

[0158] Accordingly, the EL device **2** having a configuration according to the eighth embodiment can provide the same effects as the EL device **2** having a configuration illustrated in FIG. **9**.

[0159] Moreover, in the EL device **2** according to the eighth embodiment, the main body portion TW**1** of the terminal wiring line TW (especially, a portion extending between the active region DA and the active side slit **43**) is formed from the source conductive layer **34** having a lower resistance than that of the gate conductive layer **32**. Thus, the EL device **2** according to the eighth embodiment allows a delay in data signal to reduce and in turn, ensures a large margin for design compared with the EL device **2** according to the seventh embodiment above.

[0160] Moreover, in the EL device **2** having the configuration according to the eighth embodiment, the bending slit **42** and the active side slit **43** can each include a plurality of aligned slit groups similar to the EL device **2** having the configuration according to the seventh embodiment above. The bending slit **42** including a plurality of aligned slit groups makes the EL device **2** more bendable at the bendable region **52** similar to the modified embodiment of the seventh embodiment. In addition, the active side slit **43** including a plurality of aligned slit groups allows the EL device **2** to have higher reliability similar to that of the modified embodiment of the seventh embodiment.

[0161] Alternatively, in the EL device **2** according to the eighth embodiment as well, the bending slit **42** being a

single continuous slit and the active side slit **43** including one or more aligned slit groups can be combined. The bending slit **42** being a single continuous slit can reduce an effective width of the terminal portion **51** as well as can make the EL device **2** more bendable at the bendable region **52** similar to the modified embodiment of the seventh embodiment.

Ninth Embodiment

[0162] Step S3, considered as a feature of another embodiment of the disclosure, will be described hereinafter with reference to FIGS. **20**A to **22**. Note that step S9, considered as a feature of the present embodiment, is the same as step S9 by which the second embodiment is characterized, and therefore, its description is omitted here.

[0163] FIG. **20**A is a plan view illustrating a configuration example of the EL device **2** of the ninth embodiment. FIG. **20**B is a partially enlarged view of the bendable region **52** illustrated in FIG. **20**A. FIG. **21** is a cross-sectional view taken along line A-A' of FIG. **20**A. FIG. **22** is a cross-sectional view taken along line B-B' of FIG. **20**A.

[0164] As illustrated in FIGS. **20**A and **20**B, the bending slit **42** can include a plurality of island-like slits **42'** each disposed so as to cross a corresponding terminal wiring line TW in a one-to-one correspondence instead of including a single continuous slit. For example, in a case where the bending slit **42** includes two aligned slit groups, (i) the island-like slits **42'** of one aligned slit group are aligned in the direction crossing the direction in which the terminal wiring lines TW extend, so as to cross an odd number of terminal wiring lines TW in a one-to-one correspondence and (ii) the island-like slits **42'** of the other aligned slit group are aligned in the direction crossing the direction in which the terminal wiring lines TW extend, so as to cross an even number of terminal wiring lines TW in a one-to-one correspondence, and (iii) the two aligned slit groups are arranged in the terminal wiring lines TW such that their island-like slits **42'** are disposed alternately. Hence, as illustrated in FIG. **21**, in portions between the island-like slits **42'** crossing the even-numbered terminal wiring lines TW, banks **62** are formed covering the odd-numbered terminal wiring lines TW. Likewise, in portions between the island-like slits **42'** crossing the odd-numbered terminal wiring lines TW, banks **62** are formed covering the even-numbered terminal wiring lines TW. Note that the island-like slits **42'** and the terminal wiring lines TW can cross in other than a one-to-one correspondence. Each island-like slits **42'** may cross one terminal wiring line TW, and each terminal wiring line TW may cross one or more island-like slits **42'**. For example, one terminal wiring line TW can cross several island-like slits **42'**.

[0165] Preferably, a plurality of island-like slits **42'** constituting the bending slit **42** are arranged to form a plurality of aligned slit groups adjacent in the direction in which the terminal wiring lines TW extend. In this case, the island-like slits **42'** included in different aligned slit groups can alternately cross the terminal wiring line TW. Preferably, the plurality of island-like slits **42'** constituting the bending slit **42** are arranged so as to partially overlap each other as viewed from the direction in which the terminal wiring lines TW extend. In this case, every gap between the terminal wiring lines TW is blocked by a corresponding island-like slits **42'** as viewed in the direction in which the terminal wiring lines TW extend.

[0166] Preferably, end portions (except the outermost end portion of the bending slit **42**) of the island-like slits **42'** of a plurality of aligned slit groups constituting the bending slit **42** overlap another island-like slits **42'** included in the plurality of aligned slit group when viewed in the direction in which the terminal wiring lines TW extend. Preferably, the outermost end portion of the bending slit **42** reaches the outer periphery of the EL device **2**. This prevents a crack from spreading through between the plurality of island-like slits **42'** constituting the bending slit **42**.

[0167] As illustrated in FIG. **22**, the individual island-like slits **42'** included in the bending slit **42** extend through the first inorganic insulating film **18** and the second inorganic insulating film **20**. The terminal wiring lines TW are each formed from only the gate conductive layer **32**. The terminal wiring lines TW each cross a corresponding island-like slit **42'**, passing through the bottom surface of the island-like slit **42'**. To prevent the terminal wiring line TW from being exposed, each island-like slit **42** is filled with the flattening film **21**.

[0168] As illustrated in FIGS. **20**A to **21**, the individual island-like slits **42'** included in the bending slit **42** cross a single terminal wiring line TW. The island-like slits **42'** included in the bending slit **42** are separated from one another by the banks **62** formed from the first inorganic insulating film **18** and the second inorganic insulating film **20**. The upper surface of the bank **62** is the upper surface of the second inorganic insulating film **20** so that residues of the source conductive layer **34** is less likely to remain. Even in a case where the residues of the source conductive layer **34** remains on the bottom surfaces and inner surfaces of several island-like slits **42'** included in the bending slit **42**, the residues of the source conductive layer **34** does not remain on the upper surface of the banks **62** surrounding the island-like slits **42'**. Therefore, since the configuration of the EL device **2** according to the ninth embodiment prevents the short-circuit failure through the residues of the source conductive layer **34** from occurring, it is preferred to perform etching for forming the island-like slits **42'** and etching for forming the contact hole **46** at the same time.

[0169] Other than the aforementioned points regarding the island-like slits **42'** included in the bending slit **42**, the EL device **2** according to the ninth embodiment is the same as that of the second embodiment in terms of configuration and step sequence. Thus, their descriptions are omitted here.

[0170] Also, the active side slit **43** included in the IC chip outer circumferential slit **40** can similarly include a plurality of island-like slits **43'** disposed to cross the terminal wiring lines TW in a one-to-one correspondence.

Advantageous Effects

[0171] The EL device **2** according to the ninth embodiment can provide the same effect as the EL device **2** having a configuration according to the second embodiment.

Supplement

[0172] A display device according to a first aspect of the disclosure includes: a TFT layer including a plurality of inorganic insulating films; and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The display device includes a first slit pattern and a second slit pattern each

extending through at least one of the plurality of inorganic insulating films, the first slit pattern is formed between the active region and the terminal region in plan view, and the terminal region is sandwiched between the first slit pattern and the second slit pattern in plan view.

[0173] According to a second aspect of the disclosure, the display device of the first aspect may be configured such that an IC chip is mounted on the terminal region.

[0174] According to a third aspect of the disclosure, the display device of the first or second aspect may be configured such that a flexible circuit board is connected between the second slit pattern and an edge of the display device in a plan view.

[0175] According to a fourth aspect of the disclosure, the display device of any one of the first to third aspects may be configured such that at least a part of the plurality of terminals are formed from a conductive layer above the plurality of inorganic insulating films.

[0176] According to a fifth aspect of the disclosure, the display device of any one of the first to fourth aspects may be configured such that the first slit pattern includes a continuous slit extending in a direction crossing a plurality of terminal wiring lines connected to the plurality of terminals.

[0177] According to a sixth aspect of the disclosure, the display device of the fifth aspect may further include a barrier layer below the TFT layer.

[0178] According to a seventh aspect of the disclosure, the display device of the sixth aspect may be configured such that the first slit pattern and the second slit pattern do not reach the barrier layer.

[0179] According to an eighth aspect of the disclosure, the display device of the seventh aspect may be configured such that the plurality of terminal wiring lines pass below the first slit pattern.

[0180] According to a ninth aspect of the disclosure, the display device of the eighth aspect may be configured such that the plurality of terminal wiring lines are formed in the same layer as a layer of a gate wiring of the TFT layer.

[0181] According to a tenth aspect of the disclosure, the display device of the sixth aspect may be configured such that the first slit pattern and the second slit pattern extend through the plurality of inorganic insulating films and reach the inside of the barrier layer, or extend through the plurality of inorganic insulating films and the barrier layer.

[0182] According to an eleventh aspect of the disclosure, the display device of the tenth aspect may be configured such that the plurality of terminal wiring lines pass an inner surface and a bottom surface of the first slit pattern.

[0183] According to a twelfth aspect of the disclosure, the display device of the tenth aspect may be configured such that the first slit pattern is filled with an organic insulating material, and the plurality of terminal wiring lines pass above the first slit pattern.

[0184] According to a thirteenth aspect of the disclosure, the display device of the eleventh or twelfth aspect may be configured such that a main body portion of each of the plurality of terminal wiring lines extending between the active region and the first slit pattern is formed in the same layer as a layer of the plurality of terminals.

[0185] According to a fourteenth aspect of the disclosure, the display device of the eleventh or twelfth aspect may be configured such that the plurality of terminal wiring lines include a main body portion (TW**1**) extending between the active region and the first slit pattern and a crossing portion (TW**5**) crossing the first slit pattern, and the main body portion and the crossing portion are formed from different conductive layers.

[0186] According to a fifteenth aspect of the disclosure, the display device of the eleventh or twelfth aspect may be configured such that the first slit pattern is tapered with a width of the first slit pattern being reduced toward a bottom.

[0187] According to a sixteenth aspect of the disclosure, the display device of any one of the first to fourth aspects may be configured such that the first slit pattern includes one or more aligned slit groups including a plurality of island-like slits arranged in a direction crossing the plurality of terminal wiring line connected to the plurality of terminals.

[0188] According to a seventeenth aspect of the disclosure, the display device of the sixteenth aspect may be configured such that the plurality of terminal wiring lines do not overlap the first slit pattern.

[0189] According to an eighteenth aspect of the disclosure, the display device of the seventeenth aspect may be configured such that the plurality of island-like slits of each of the one or more aligned slit groups are arranged with the plurality of terminal wiring lines pass between the plurality of island-like slits of each of the one or more aligned slit groups in a one-to-one correspondence.

[0190] According to a nineteenth aspect of the disclosure, the display device of the sixteenth aspect may be configured such that the plurality of island-like slits each cross only one of the plurality of terminal wiring lines.

[0191] According to a twentieth aspect of the disclosure, the display device of the nineteenth aspect may be configured such that the plurality of island-like slits are arranged while crossing the plurality of terminal wiring lines in a one-to-one correspondence.

[0192] According to a twenty-first aspect of the disclosure, the display device of any one of the seventeenth to twentieth aspects may be configured such that a barrier layer is provided below the TFT layer, and the first slit pattern extends through the plurality of inorganic insulating films and reach the inside of the barrier layer, or extends through the plurality of inorganic insulating films and the barrier layer.

[0193] According to a twenty-second aspect of the disclosure, the display device of any one of the sixteenth to twenty-first aspects may be configured such that the first slit pattern includes a plurality of island-like slit groups, and the plurality of island-like slits included in the plurality of island-like slit groups are arranged in a staggered manner in plan view while not forming a gap between the plurality of island-like slits as viewed from a direction in which the plurality of terminal wiring lines extend.

[0194] According to a twenty-third aspect of the disclosure, the display device of the twenty-second aspect may be configured such that an end of an island-like slit included in the plurality of island-like slits overlaps another island-like slit of the plurality of island-like slits as viewed from a direction in which the plurality of terminal wiring lines extend.

[0195] According to a twenty-fourth aspect of the disclosure, the display device of any one of the fifth to twenty-third aspects may be configured such that the terminal region is surrounded by the first slit pattern, the second slit pattern including a continuous slit, and two fourth slit patterns

including a continuous slit extending in the same direction as the plurality of terminal wiring lines.

[0196] According to a twenty-fifth aspect of the disclosure, the display device of any one of the fifth to twenty-fourth aspects may be configured such that a bendable region is formed between the active region and the first slit pattern, and a third slit pattern is formed in the bendable region while extending through at least one of the plurality of inorganic insulating films.

[0197] According to a twenty-sixth aspect of the disclosure, the display device of the twenty-fifth aspect may be configured such that the first slit pattern and the third slit pattern have the same depth.

[0198] According to a twenty-seventh aspect of the disclosure, the display device of the twenty-sixth aspect may be configured such that the first slit pattern and the third slit pattern have the same slit pattern.

[0199] According to a twenty-eighth aspect of the disclosure, the display device of the twenty-sixth or twenty-seventh aspect may be configured such that a barrier layer is provided below the TFT layer, a support member is provided below the barrier layer, the first slit pattern and the third slit pattern extend through the plurality of inorganic insulating films and the barrier layer, reach the support member, and also are filled with an organic insulating material, and the plurality of terminal wiring lines pass above the organic insulating material.

[0200] According to a twenty-ninth aspect of the disclosure, the display device of any one of the twenty-fifth to twenty-eighth aspects may include a sealing layer covering the light emitting element layer. The display device is of an upward light emission type device configured to allow light emitted from the light emitting element layer to pass through the sealing layer and is bent along the third slit pattern as a hold with the surface of the plurality of terminals facing downward.

[0201] According to a thirtieth aspect of the disclosure, the display device of any one of the fifth to twenty-ninth aspect may be configured such that at least a part of the plurality of terminal wiring lines is formed from a conductive layer above the plurality of inorganic insulating films and also covered with an organic insulating film above the TFT layer.

[0202] According to a thirty-first aspect of the disclosure, the display device of any one of the first to thirtieth aspects may include a flexible support member.

[0203] A method for manufacturing a display device according to a thirty-second aspect of the disclosure is a method for manufacturing a display device including a TFT layer including a plurality of inorganic insulating films and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The method including: forming a first slit pattern extending through at least one of the plurality of inorganic insulating films, between the active region and the terminal region in plan view; and forming a second slit pattern extending through at least one of the plurality of inorganic insulating films so as to sandwich the terminal region together with the first slit pattern in plan view.

[0204] According to a thirty-third aspect of the disclosure, the method for manufacturing a display device of the thirty-second aspect may be such that a third slit pattern extending through at least one of the plurality of inorganic insulating films is formed between the active region and the first slit pattern.

[0205] According to a thirty-fourth aspect of the disclosure, the method for manufacturing a display device of thirty-third aspect may be such that the first slit pattern and the third slit pattern are formed through the same process.

[0206] According to a thirty-fifth aspect of the disclosure, the method for manufacturing a display device of any one of the thirty-second to thirty-fourth aspects may be such that an electronic circuit board is mounted on the terminal region by thermocompression bonding.

[0207] According to a thirty-sixth aspect of the disclosure, the method for manufacturing a display device of the thirty-third or thirty-fourth aspect may be such that the display device is bent along the third slit pattern so that the terminal region is provided on the rear side.

[0208] A manufacturing apparatus configured to manufacture a display device according to a thirty-seventh aspect of the disclosure is a manufacturing apparatus configured to manufacture a display device including a TFT layer including a plurality of inorganic insulating films and a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region. The manufacturing apparatus is configured to form a first slit pattern extending through at least one of the plurality of inorganic insulating films, between the active region and the terminal region in plan view, and to form a second slit pattern extending through at least one of the plurality of inorganic insulating films while sandwiching the terminal region together with the first slit pattern in plan view.

Additional Items

[0209] The disclosure is not limited to the embodiments stated above. Embodiments obtained by appropriately combining technical approaches stated in each of the different embodiments also fall within the scope of the technology of the disclosure. Moreover, novel technical features may be formed by combining the technical approaches stated in each of the embodiments.

[0210] For example, the technical scope of the disclosure encompasses a configuration obtained by combining the configuration according to the first embodiment and the configuration according to the fourth embodiment as illustrated in FIG. **23**.

[0211] FIG. **23** is a cross-sectional view illustrating a configuration example obtained by combining the configuration in which the gate conductive layer **32** is exposed at the bottom surface of the IC chip outer circumferential slit **40** of the EL device **2** (see FIG. **5**) according to the first embodiment and the configuration of the EL device **2** (see FIG. **11**) according to the fourth embodiment at the bendable region **52** and its surroundings. The bending slit **42** of FIG. **23** extends through the inorganic barrier layer **3**, the gate conductive layer **32**, and the plurality of inorganic insulating films **16**, **18**, and **20**. The active side slit **43** and the FPC side slit **44** of FIG. **23** extend through the first and second inorganic insulating films **18** and **20**.

REFERENCE SIGNS LIST

[0212] **2** EL device

[0213] **4** TFT layer

[0214] **3** Inorganic barrier film (barrier layer)
[0215] **5** Light emitting element layer
[0216] **6** Sealing layer
[0217] **7** Layered body
[0218] **8**, **11** Adhesive layer
[0219] **9** Protection member
[0220] **10** Support member
[0221] **12** Resin layer (flexible support member)
[0222] **13** Peeling layer
[0223] **15** Semiconductor layer
[0224] **16** Gate insulating film
[0225] **16**, **18**, **20** Inorganic insulating film
[0226] **21** Flattening film
[0227] **22** Anode electrode
[0228] **23** Bank layer
[0229] **23***b* Bank
[0230] **23***c* Partition
[0231] **24** EL layer
[0232] **25** Cathode electrode
[0233] **26** First inorganic sealing film
[0234] **26**, **28** Inorganic sealing film
[0235] **27** Organic sealing film
[0236] **28** Second inorganic sealing film
[0237] **32** Gate conductive layer
[0238] **34** Source conductive layer
[0239] **36** Intermediate conductive layer
[0240] **32**, **34**, **36** Conductive layer
[0241] **38** Buried material (organic insulating material)
[0242] **40** IC chip outer circumferential slit
[0243] **42** Bending slit (third slit pattern)
[0244] **42'** Island-like slit
[0245] **43** Active side slit (first slit pattern)
[0246] **43'** Island-like slit
[0247] **44** FPC side slit (second slit pattern)
[0248] **45** End side slit (fourth slit pattern)
[0249] **46** Contact hole
[0250] **50** Mother substrate
[0251] **51** Terminal portion
[0252] **52** Bendable region (bending region)
[0253] **56** IC chip mounted region (terminal region)
[0254] **58** FPC connection region
[0255] **60** Slit
[0256] **62** Bank
[0257] DA Active region
[0258] NA Non-active region
[0259] TM, TM**1**, TM**2** Terminal
[0260] TW Terminal wiring line
[0261] TW**1** Main body portion
[0262] TW**2** Active side portion
[0263] TW**3** Terminal side portion
[0264] TW**4** Bending slit bridge portion (crossing portion)
[0265] TW**5** Outer circumferential slit bridge portion (crossing portion)

1. A display device comprising:
a TFT layer including a plurality of inorganic insulating films; and
a light emitting element layer above the TFT layer, the TFT layer including a terminal region including a plurality of terminals, the terminal region being provided outside an active region,
wherein the display device includes a first slit pattern and a second slit pattern each extending through at least one of the plurality of inorganic insulating films,
the first slit pattern is formed between the active region and the terminal region in plan view, and
the terminal region is sandwiched between the first slit pattern and the second slit pattern in plan view.

2. The display device according to claim **1**,
wherein an IC chip is mounted on the terminal region.

3. The display device according to claim **1**,
wherein a flexible circuit board is connected between the second slit pattern and an edge of the display device in plan view.

4. The display device according to claim **1**,
wherein at least a part of the plurality of terminals is formed from a conductive layer above the plurality of inorganic insulating films.

5. The display device according to claim **1**,
wherein the first slit pattern includes a continuous slit extending in a direction crossing a plurality of terminal wiring lines connected to the plurality of terminals.

6. The display device according to claim **5** further comprising:
a barrier layer below the TFT layer.

7. The display device according to claim **6**,
wherein the first slit pattern and the second slit pattern do not reach the barrier layer.

8. The display device according to claim **7**,
wherein the plurality of terminal wiring lines pass below the first slit pattern.

9. The display device according to claim **8**,
wherein the plurality of terminal wiring lines are formed in the same layer as a layer of a gate wiring line of the TFT layer.

10. The display device according to claim **6**,
wherein the first slit pattern and the second slit pattern extend through the plurality of inorganic insulating films and reach an inside of the barrier layer, or extend through the plurality of inorganic insulating films and the barrier layer.

11. The display device according to claim **10**,
wherein the plurality of terminal wiring lines pass an inner surface and a bottom surface of the first slit pattern.

12. The display device according to claim **10**,
wherein the first slit pattern is filled with an organic insulating material, and the plurality of terminal wiring lines pass above the organic insulating material.

13. The display device according to claim **11**,
wherein a main body portion of each of the plurality of terminal wiring lines extending between the active region and the first slit pattern is formed in the same layer as a layer of the plurality of terminals.

14. The display device according to claim **11**,
wherein the plurality of terminal wiring lines include a main body portion extending between the active region and the first slit pattern and a crossing portion crossing the first slit pattern, and
the main body portion and the crossing portion are formed from different conductive layers.

15. The display device according to claim **11**,
wherein the first slit pattern is tapered with a width of the first slit pattern being reduced toward a bottom.

16. The display device according to claim **1**,
wherein the first slit pattern includes one or more aligned slit groups including a plurality of island-like slits

arranged in a direction crossing the plurality of terminal wiring lines connected to the plurality of terminals.

17. The display device according to claim **16**,

wherein the plurality of terminal wiring lines do not overlap the first slit pattern.

18. The display device according to claim **17**,

wherein the plurality of island-like slits of each of the one or more aligned slit groups are arranged with the plurality of terminal wiring lines passing between the plurality of island-like slits constituting each of the one or more aligned slit groups in a one-to-one correspondence.

19-23. (canceled)

24. The display device according to claim **5**,

wherein the terminal region is surrounded by the first slit pattern, the second slit pattern including a continuous slit, and two fourth slit patterns including a continuous slit extending in the same direction as the plurality of terminal wiring lines.

25. The display device according to claim **5**,

wherein a bendable region is formed between the active region and the first slit pattern, and

a third slit pattern is formed in the bendable region and extends through at least one of the plurality of inorganic insulating films.

26-37. (canceled)

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摘要(译)

有源侧狭缝和FPC侧狭缝均延伸穿过第二无机绝缘膜并到达第一无机绝缘膜。 在平面图中,有源侧缝隙形成在EL器件的有源区和IC芯片安装区之间,并且,IC芯片安装区夹在有源侧缝隙和FPC侧缝隙之间。